TOOLS TO ASSESS THE ATTACHMENT RELIABILITY OF MODERN SOLDERED ASSEMBLIES (BGA, CSP...)

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Abstract

This paper discusses design and material issues that affect the reliability of perimeter PBGA and CSPs assemblies. Related tools have been implemented in a PC-based application that allows for rapid assessment of the complex effects of package geometry and material properties on solder joint reliability.

Introduction

Design trends that impact the attachment reliability of modern, high density miniaturized electronic assemblies include:

- Increased silicon contents and/or package size -- resulting in a possibly large CTE[1] mismatch between component and board.
- Lower profile constructions with reduced stand-off height and increased stiffness.
- Smaller size solder joints with less load bearing and crack propagation area than conventional Surface Mount (SM) interconnects.

The implied reliability risks are application-specific and depend on a large number of parameters: assembly quality, solder metallurgy, individual board and package constructions, die size, field use conditions and the intended design life of the product. Risk levels are possibly higher for fine-pitch, low-profile IC[2] packages, BGA[2] and CSP[2] assemblies than for conventional packages with tall compliant leads. For example, life limiting guidelines have been suggested for some full-array PBGAs[3] and Alloy42 TSOPs[3] in computer and telecommunication applications [1, 2]. The same packages would have adequate reliability margins under other, more benign conditions. Given the above risk factors, the attachment integrity of BGA and CSP constructions needs to be looked at carefully and evaluated on a case-by-case basis. Solder joint life prediction techniques have been developed that allow physical designers to assess attachment reliability in the early stages of product development (see [3,4], for example). This paper presents recent applications of the Solder Reliability Solutions (SRS) model [4] to perimeter PBGA and CSP assemblies.

Model Overview

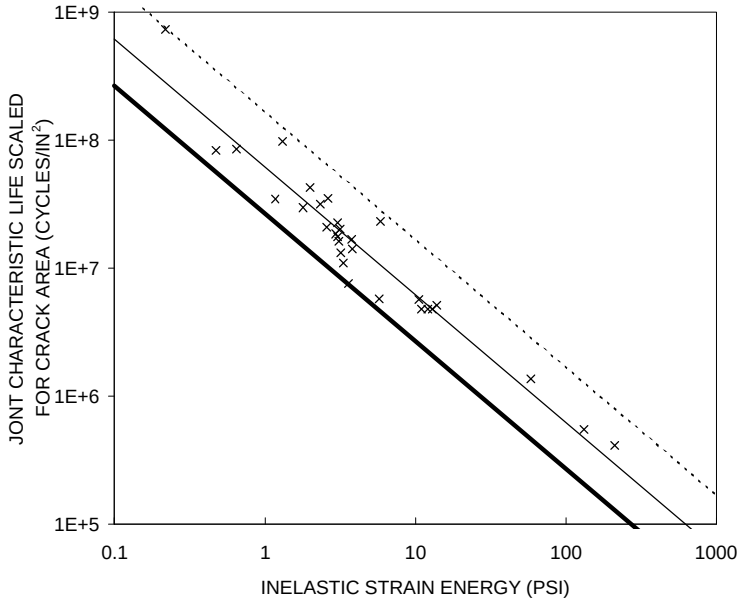

Figure 1: SRS correlation of test data (30 experiments).

[1]CTE= Coefficient of Thermal Expansion.

[2]IC = Integrated Circuit; BGA = Ball Grid Array; CSP = Chip Scale Package.

[3]PBGA = Plastic Ball Grid Array; TSOP =Thin Small Outline Package.

The early version of SRS was developed for conventional surface mount assemblies (discrete chips, peripheral leadless and leaded packages) and full array PBGAs [4, 5]. Package modeling capabilities have since been extended to popular CSPs (flip-chip with underfill, micro-BGAs) [4, 6] and, more recently, to perimeter PBGAs. The physical models account for plastic flow and creep of solder, and include local CTE mismatch effects and failure statistics. Structural analysis of board/component interactions uses simplified, one-dimensional engineering mechanics models. The analysis, presented in [4-6], includes stretching and bending of parts for leadless assemblies, and flexural stiffness parameters for leaded components. The correlation of accelerated test data uses inelastic strain energy as a measure of cyclic damage (Fig. 1). On the vertical axis, the joint characteristic life scaled for the solder crack area is the inverse of a two-dimensional crack propagation rate in cycles/in^2. The fatigue life model has been validated over a wide range of test conditions and for common families of components assembled with eutectic or near-eutectic Sn-Pb. The data is from 30 experiments and covers three orders of magnitude along the x- and y-axis.

PBGA Assemblies

Full Array PBGAs

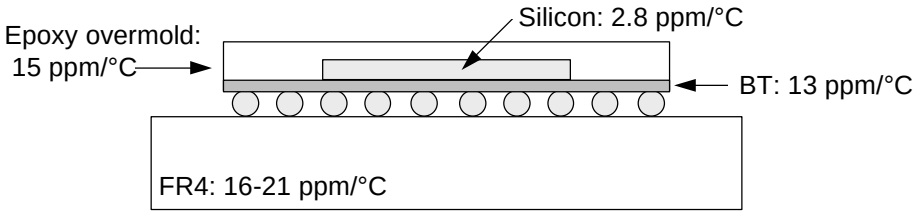

Figure 2: Schematic of full array PBGA assembly.

The effects of package geometry and material properties on solder joint fatigue in full array PBGA assemblies (Fig. 2) are fairly well understood [7]. Main factors that impact assembly reliability include die size and thickness, BT thickness, solder attach pad area (and pad configuration), and component stand-off height. On organic boards with a large CTE (say 16 to 21 ppm/ºC), joints under the edge of the die are likely to fail first because of the low effective CTE of the package in the die area. Note, however, that *failure conditions are expected to be different on low expansion boards* -- where the die area would be better CTE-matched to the substrate -- and each design needs be evaluated on an individual basis.

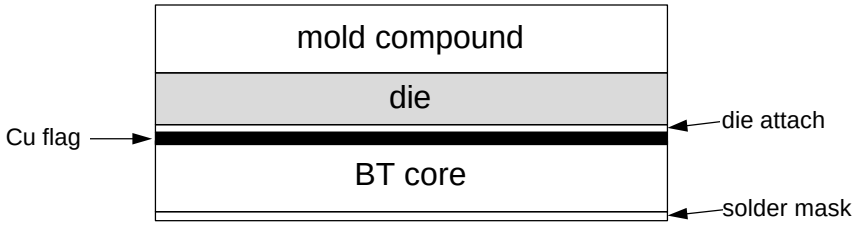

Figure 3: Multi-layer construction in die area.

The SRS tool uses classical thermal stress analysis of multi-layer stacks to predict the effective package CTE in the die area. The analysis [4, 8] accounts for stretching, flexing and thermal expansion of individual layers in a multi-layer construction (Fig. 3) subject to a uniform temperature swing. The validation of the full array PBGA model against accelerated test data was demonstrated in [4, 5, 9]. In the next section, the full array model is expanded to perimeter PBGAs.

Perimeter PBGA Model

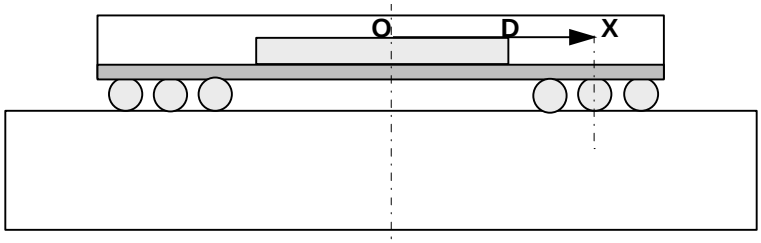

Figure 4: Schematic of perimeter PBGA assembly;
O = neutral point, D = die corner, X = Distance to Neutral Point (DNP).

Intuitively, the low expansivity of silicon (CTE~2.8 ppm/ºC) still influences the global CTE mismatch in perimeter PBGA assemblies (Fig. 4). The effective package CTE at the first inner row of joints may be better matched to FR4 than in full array assemblies because the solder mask, the BT substrate and the package molding compound have higher CTEs than silicon. Local CTE mismatch between the solder joints and the package -- an important contributor to solder joint fatigue under the edge of the die in full array PBGAs [3, 7] -- is also greatly reduced because there is no silicon directly above the solder joints. Thus, everything else being equal in terms of geometry and materials, perimeter PBGAs are potentially more reliable than full array PBGAs on conventional FR4 boards. These conclusions are supported by preliminary experimental studies in [10].

Using a lumped parameter approach, the effective global CTE of the package, $\alpha_G(L)$, at the bottom of the perimeter PBGA and at a distance X = L from the neutral axis is obtained by adding the thermal expansions of the bottom fibers of the package in the die area and beyond the edge of the die, that is:

$$L\alpha_G(L)\Delta T = L_D\alpha_D\Delta T + (L - L_D)\alpha_M\Delta T \qquad (1)$$

where ΔT is the temperature swing, α_D is the effective composite CTE in the die area, L_D is the die maximum DNP (half-diagonal length) and α_M is the effective composite CTE beyond the edge of the die. The effective composite CTEs (α_D and α_M) are obtained from total strains at the bottom of each multilayer region (die area and region beyond the edge of the die) using Hall's thermo-mechanical model of multilayer structures [8]. From (1), the effective global CTE at the bottom of the package is:

$$\alpha_G(L) = \alpha_D \frac{L_D}{L} + \alpha_M \frac{(L - L_D)}{L} \qquad (2)$$

Perimeter PBGA Example

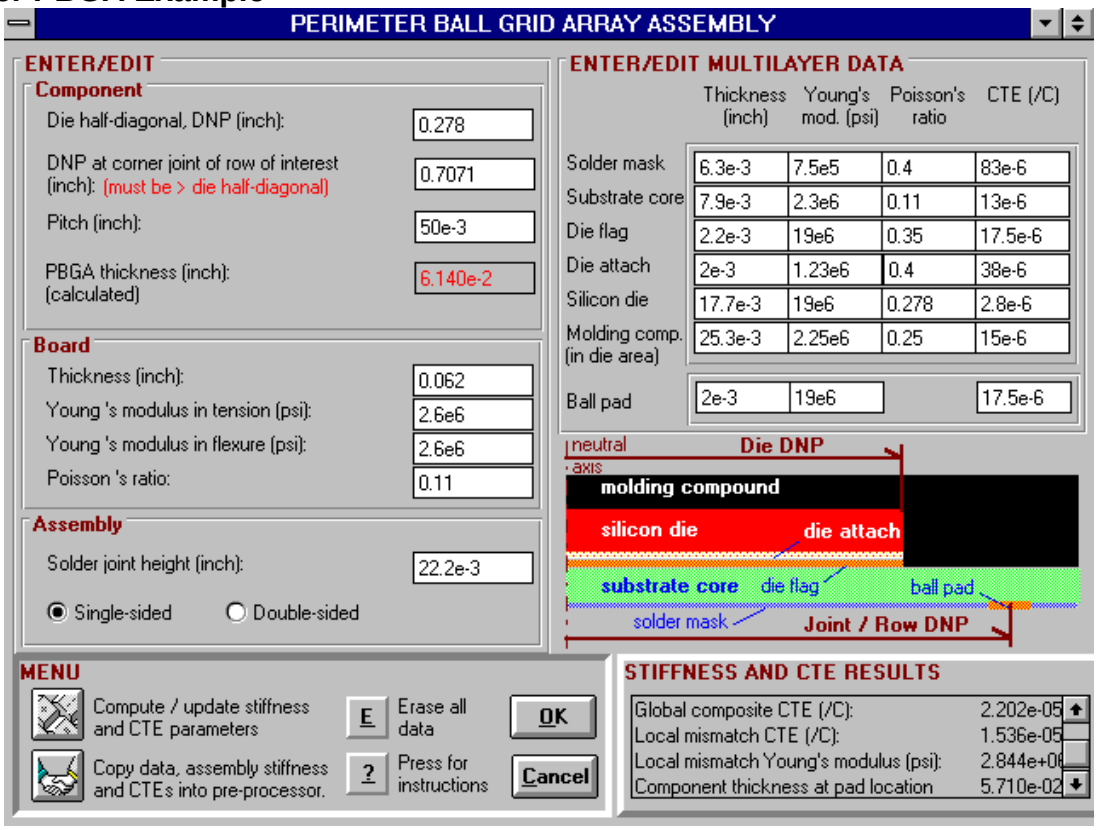

Figure 5: Model input data for 256 I/O perimeter PBGA example.

Consider a 10 mm square die (L_D = 0.278") in a 4 row, 1.27 mm pitch, 256 I/O perimeter PBGA with material properties and geometric parameters given in Figure 5. Computed effective global CTEs in the package diagonal direction are tabulated below:

Row number	Corner joint DNP (inch)	α_G (ppm/ºC)
1 (inner row)	0.495	19.31
2	0.5657	20.44
3	0.6364	21.32
4 (outer row)	0.7071	22.02

Since the first row of joints is relatively far from the edge of the die (L = 0.495" for row # 1 vs. L_D = 0.278" at the corner of the die), differences in α_G between the inner and outer rows are slight. Nevertheless, this can result in subtle differences in failure modes depending on the CTE of the motherboard. For example, for a board CTE of 18 ppm/ºC, the maximum global CTE mismatch would be at the outer row ($\Delta\alpha$ = 22.02 -18 = 4.02 ppm/ºC), whereas for a larger board CTE of 21.5 ppm/ºC, the maximum CTE mismatch would be at the inner row ($\Delta\alpha$ = 21.5 - 19.31 = 2.19 ppm/ºC). These CTE mismatches are lower than those encountered at the edge of the die in full array PBGA assemblies and higher attachment reliability is still expected.

The input data for reliability analysis includes no less than 35 parameters (white text boxes in Fig. 5), from die size to CTE, modulus, Poisson's ratio and thickness of the individual material layers in the package construction. The above example highlights the complexity of the problem and suggests that geometric dimensions and measurement of material properties are important ingredients of the reliability assessment process.

CSP Assemblies

Because of the large silicon contents of CSPs, their attachment reliability on organic boards is inherently at risk unless special design features are built-in to provide structural compliance and/or to decouple the die from the board. This design philosophy is the guiding principle behind flip-chip with underfill and micro-BGA assemblies. The impact of geometry and material properties on the reliability of these two types of assemblies is discussed below.

Flip-Chip with Underfill

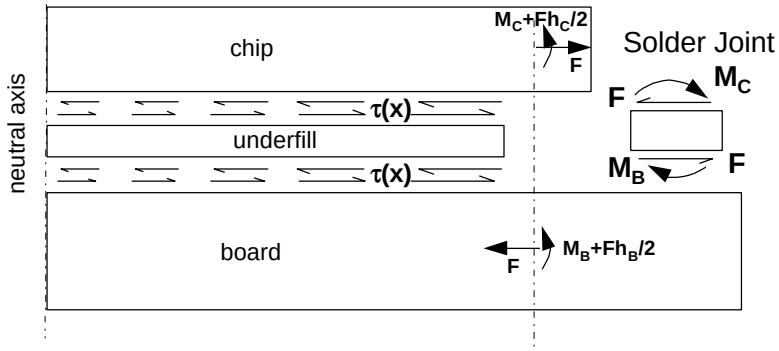

Figure 6: Interfacial shear stresses at die/underfill/substrate interfaces.

The solder joint life improvement mechanism in flip-chip assemblies with underfill is that the in-plane thermal expansion mismatch between the die and substrate is taken up by shear of the solder joints and of the underfill layer. Thus, the solder joints see lesser strains than in bare chip assemblies. A strength of materials model (see details in [6]) was developed to quantify these effects. The model gives the distribution of interfacial stresses (τ(x) in Fig. 6) along the die/underfill/substrate interfaces as well as shear forces (F) and bending moments (M's) exerted by the solder joints on the die and substrate. A solder joint strain reduction factor and an effective global CTE mismatch between the die and substrate are determined based on the relative distribution of stress in the joints and in the underfill layer.

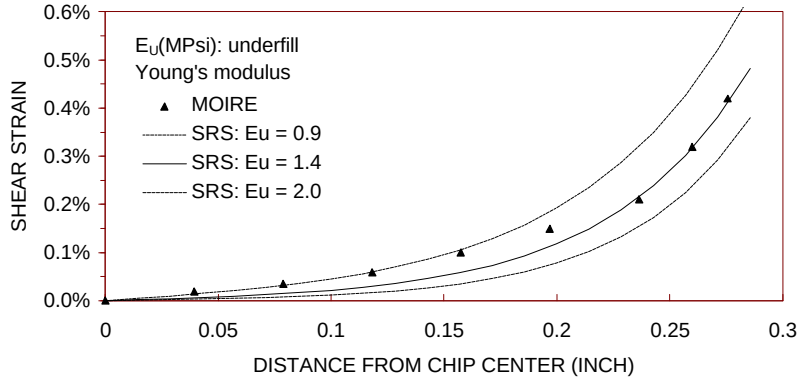

Figure 7: Measured and predicted shear strain distribution in underfill layer of silicon-on-ceramic test vehicle (ΔT= -80ºC) [11].

The model was verified by comparing predicted shear strains in the underfill layer and shear strains obtained by high sensitivity moiré analysis [11] (Fig. 7). The model is sensitive to the underfill modulus, E_U, since increased stiffening of the underfill layer provides for better coupling between the die and substrate. In the

high strain region, the model fits the data best for E_U = 0.9 Mpsi. The agreement between predictions and experiment is good and gives support to use of the model for further parametric studies. The model was also used to study underfill delamination [6]. Maximum shear stresses in the underfill layer were found to correlate with cycles-to-failure when underfill delamination was the dominant failure mode.

As an application of the underfill model, parametric studies were conducted for a generic flip-chip assembly with a 15 mil thick die on 62 mil thick FR-4 ($E=2.5x10^6$ psi, ν=0.28, CTE=16 ppm/ºC). The underfill thickness is 4 mil. Figure 8 shows the effective CTE mismatch that is achieved and maximum interfacial shear stresses (ΔT=100ºC) as a function of the underfill modulus for a 10 mm square die. For E_U = 0.4 Mpsi, the effective CTE mismatch is less than 0.975 ppm/ºC. Since the CTE mismatch for the bare chip assembly is 13.2 ppm/ºC, the strain reduction factor is R = 13.5. As the modulus increases, the strain reduction factor increases further and so does the maximum shear stress. Curves like those in Figure 8 are of use to determine a suitable range of underfill moduli for a given application.

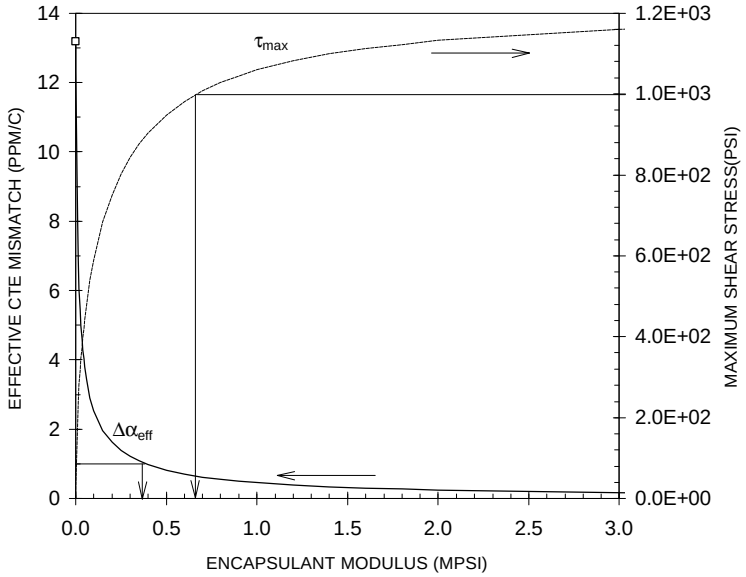

Figure 8: Effect of underfill modulus on effective CTE mismatch and maximum shear stress.

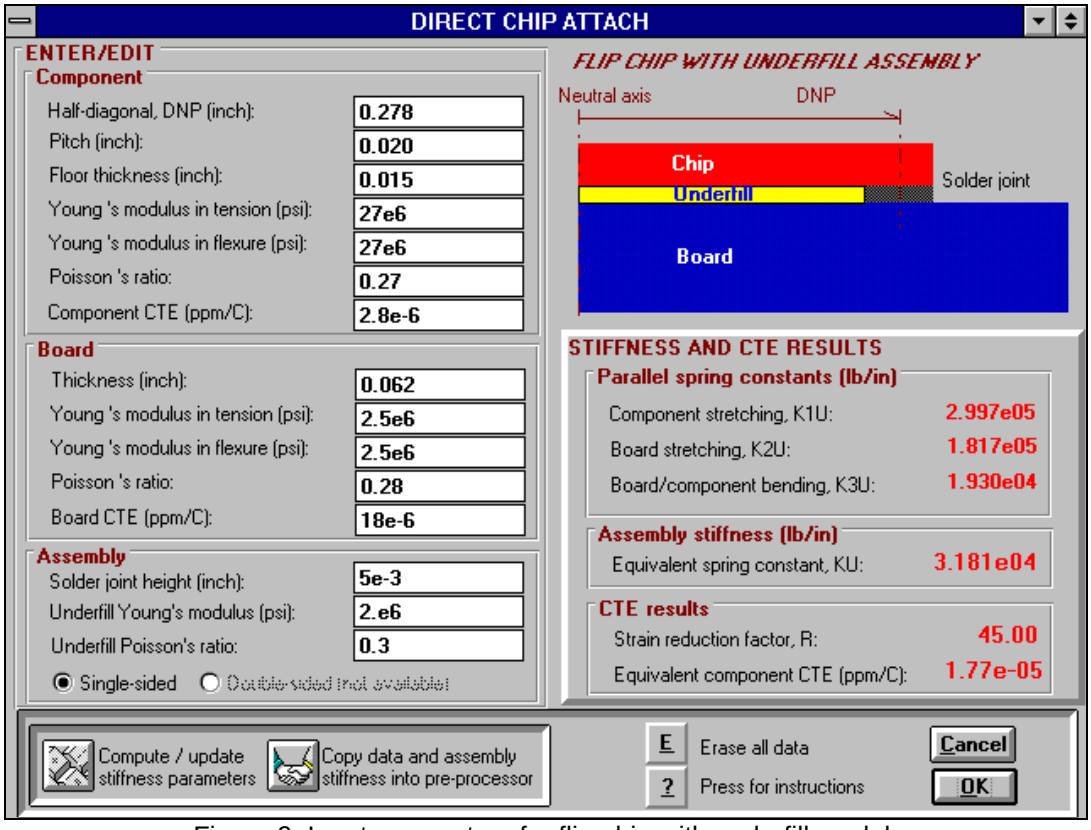

Figure 9: Input parameters for flip-chip with underfill model.

Other examples of parametric studies, such as chip size effects, can be found in [6]. Geometric dimensions and material properties for the flip-chip with underfill model total a minimum of 15 parameters (Fig.9). Other input data such as statistical parameters are required for full fledge reliability predictions. Again, the large number of parameters involved testifies to the complexity of the problem and the importance of material characterization.

Micro-BGA

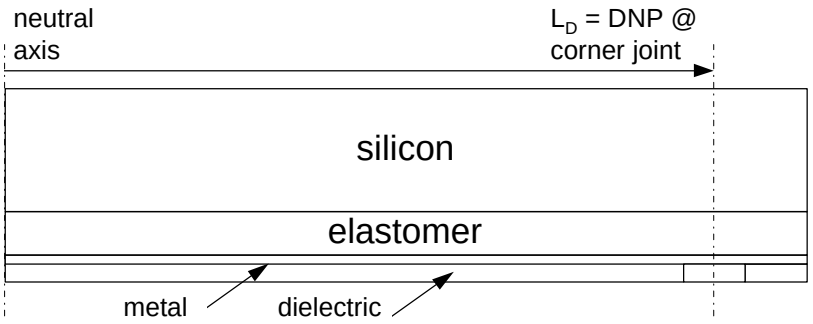

Figure 10: Schematic of micro-BGA package model.

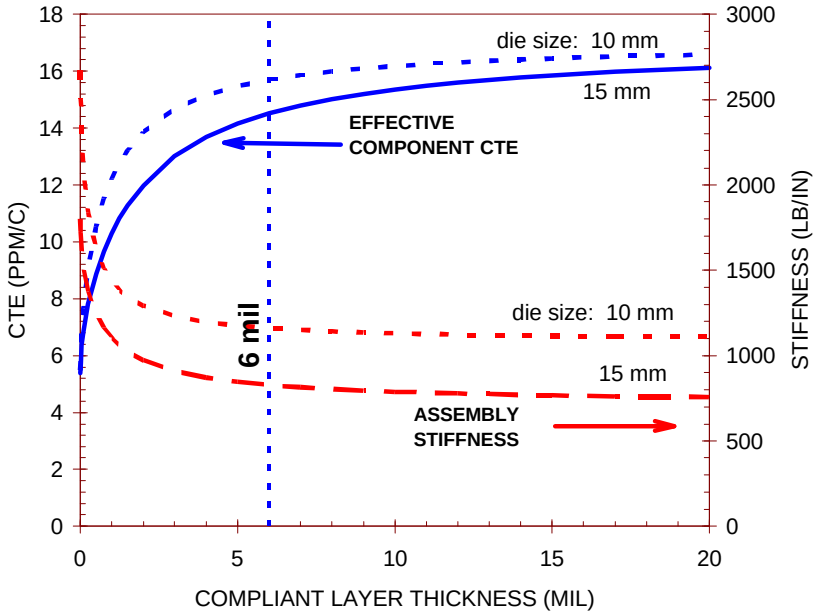

Figure 11: Micro-BGA effective CTE and assembly stiffness vs. elastomer thickness.

Figure 10 is a schematic of half of a micro-BGA package (from the neutral axis to the edge of the package). The solder joint life improvement feature is a low modulus compliant elastomer layer that provides for thermo-mechanical decoupling between the silicon die and the package substrate (metal layers + dielectric). During thermal cycling, the compliant elastomer layer, with a low modulus of a few hundred psi's, is essentially in shear and absorbs the CTE mismatch between the die and the package substrate. The thin substrate provides for added compliance of the soldered micro-BGA assembly. These effects are quantified in a model that uses stress analysis techniques similar to those of the flip-chip with underfill model. The effective package CTE that is seen by the solder joints is derived from calculated strains on the bottom side of the package. The assembly stiffness accounts for stretching and bending of the package (and the motherboard) and is obtained as a function of chip size, geometry and properties of the different material layers in the micro-BGA package.

The micro-BGA model was applied to a generic micro-BGA on 0.062" FR4 and with a 15 mil thick die. Material properties that were used are from [12]. Figure 11 shows the effective package CTE and assembly stiffness as a function of thickness of the compliant elastomer layer. The effective package CTE increases and the assembly stiffness decreases as the elastomer thickness increases. The elastomer layer has to be thick enough to provide an effective package CTE that is close to that of FR-4 boards. For a 6 mil thickness, the effective CTE is in the range 15.7 ppm/C (10 mm die) to 14.5 ppm/C (15 mm die). Beyond 6 mils, incremental gains in effective CTE and assembly compliance are limited. Nevertheless, with a minimum thickness of the

elastomer layer, the package-to-board CTE mismatch and the assembly stiffness are greatly reduced when compared to bare chips on FR-4.

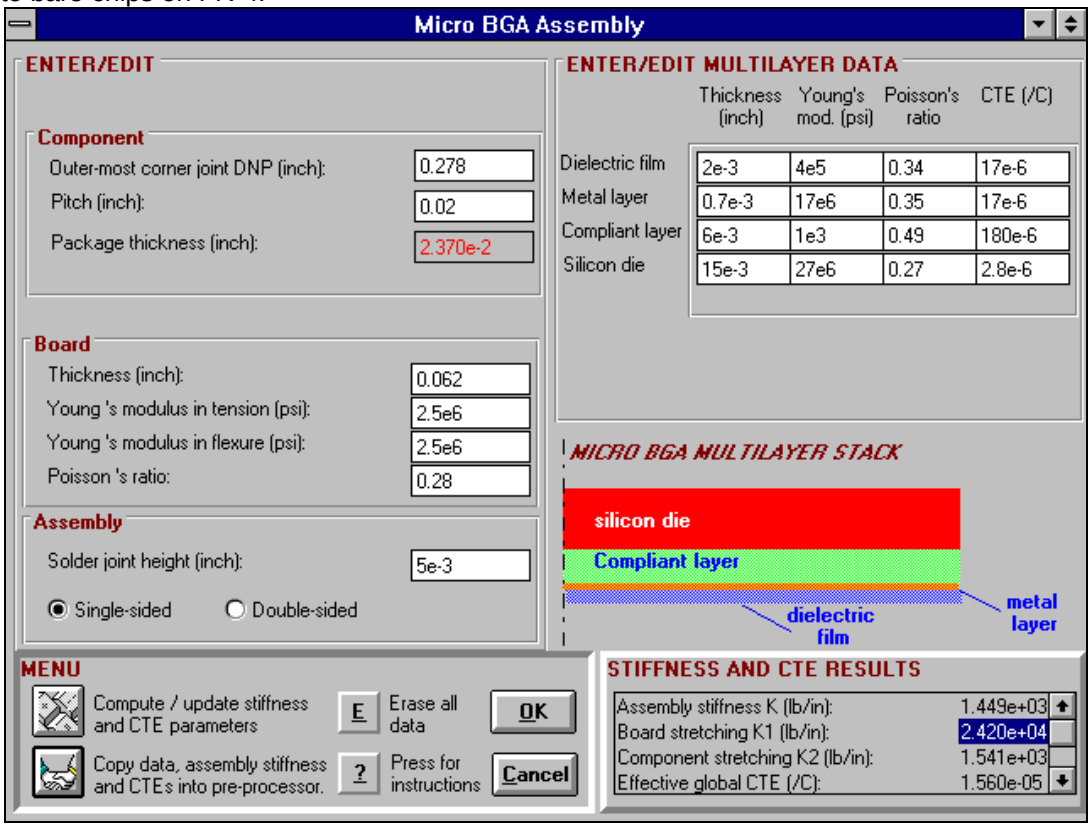

Figure 12: Input parameters of micro-BGA model.

Results of the above parametric study are in agreement with the conclusions of finite element studies in [12, 13] and suggest that the micro-BGA model quantifies the chip-to-board decoupling well. Users of the SRS software have also indicated that the micro-BGA CTE predictions are in good agreement with measured CTEs. Further verification of the micro-BGA model will be conducted as assembly reliability data becomes available. The number of input data required for model verification and/or calibration totals a minimum of 23 parameters (Fig. 12).

Conclusions

Physical models of PBGA and CSP assemblies have been developed that capture the main effects of package geometry and material properties on attachment reliability. The models have been implemented in a PC-based design-for-reliability tool that enables quick parametric studies of critical package and board properties. Given the large number of parameters involved -- one to three dozens depending on the package type -- and geometric / material variations that are unique to each design, attachment reliability of PBGAs and CSPs needs to be evaluated on a case-by-case basis.

Acknowledgments

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References

[1] M. Petrucci, R. Johnson, A. Mawer, T. McQuiggin, B. Nelson and D. Rosckes, “Feasibility Study of Ball Grid Array Packaging”, *Proceedings, Nepcon East ‘93*, Boston, MA, June 1993.

[2] D. M. Noctor, F. E. Bader, A. P. Viera, P. Boysan, S. Golwalker and D. Foehringer, "Attachment Reliability Evaluation and Failure Analysis of Thin Small Outline Packages (TSOP’s) with Alloy 42 Leadframes," *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, Vol. 16, No. 8, Dec. 1993, pp. 961-971.

[3] R. Darveaux, K. Banerji, A. Mawer and G. Dody, “Reliability of Plastic Ball Grid Array Assembly”, Chapter 13, *Ball Grid Array Technology*, ed. J. H. Lau, McGraw Hill, NY, 1995, pp. 379-442.

[4] J-P. Clech, “Solder Reliability Solutions: a PC-Based Design-For-Reliability Tool”, *Proceedings, Surface Mount International Conference*, San Jose, CA, Sept. 10-12,1996, Vol. I, pp. 136-151.

[5] J-P. Clech, “Solder Reliability Solutions: form LCCCs to area array assemblies”, *Proceedings, Nepcon West ‘96*, Anaheim, CA, Feb. 1996, pp. 1665-1680.

[6] J-P. Clech, “Reliability Challenges and Modeling of Modern Soldered Assemblies”, to appear in *Proceedings, TMS ‘97 Annual Meeting*, Orlando, FL, Feb. 9-13, 1997.

[7] R. Darveaux and A. Mawer, “Thermal and Power Cycling Limits of Plastic Ball Grid Array (PBGA) Assemblies”, *Proceedings, Surface Mount International Conference*, San Jose, CA, Aug. 29-31, 1995, pp. 315-326.

[8] P. M. Hall, “Thermal Expansivity and Thermal Stress in Multilayered Structures”, Chapter 2, *Thermal Stress and Strain in Microelectronic Packaging*, ed. J. H. Lau, Van Nostrand Reinhold, NY, 1993, pp. 78-94.

[9] T. Ejim and J-P. Clech, “Moiré Analysis and Modeling of Area Array Assemblies”, in post-conference *Proceedings, 1996 VIII International Congress on Experimental/Numerical Mechanics in Electronic Packaging*, Nashville, TN, June 1996, Society for Experimental Mechanics, Bethel, CT.

[10] C. Ramirez and S. Fauser, “Fatigue Life Comparison of the Perimeter and Full Plastic Ball Grid Array”, *Journal of Surface Mount Technology*, SMTA, July 1995, pp. 27-36.

[11] B. Han, Y. Guo and C. K. Lim “Application of Interferometric Techniques to Verification of Numerical Models for Microelectronics Packaging Design”, *Advances in Electronic Packaging, InterPack ‘95*, Maui, Hawaii, March 26-30, 1995, ASME, EEP-Vol. 10-2, pp 1187-1194.

[12] J. Fjelstad and M. Perry, “Finite Element Analysis of a Compliant Chip Scale Ball Grid Array Package”, *Proceedings, CHIPCON ’96*, February 1996.

[13] J. Fjelstad, T. DiStefano and M. Perry, “Compliancy Modeling of an Area Array Chip Scale Package”, *Proceedings, Surface Mount International*, San Jose, CA, Sept. 10-12, 1996, Vol. I, pp. 236-243.