

# SOLDER RELIABILITY SOLUTIONS: FROM LCCCS<sup>1</sup> TO AREA-ARRAY ASSEMBLIES.

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**Abstract** -- Advances in electronics packaging are placing more demand on solder interconnect reliability. For example, solder joints of leadless Ball Grid Array (BGA) and Chip-Scale Packaging (CSP) assemblies are more susceptible to early wear-out than solder joints in compliant, CTE<sup>2</sup>-matched leaded assemblies. Establishing the reliability of area-array assemblies requires robust design and assembly practices, including high yield and quality solder interconnects, characterization of package and board materials, evaluation of the structural response of the entire assembly. This paper reviews related historical trends and presents a new PC-based design-for-reliability model, Solder Reliability Solutions (SRS), that enables quick estimates of solder interconnect reliability and rapid "what-if" analysis of design parameters and material properties. The main features of the model and input data are presented in detail. The model is validated across a database of accelerated test results covering several generations of packaging and assembly technologies. Application to 225 I/O Plastic BGA (PBGA) assemblies is in good agreement with both experimental results and finite element modeling, thus enabling the rapid assessment and optimization of other area array designs.

## INTRODUCTION

Area array packaging and assembly have created new solder reliability problems requiring new solutions. This paper presents engineering modeling techniques and a computer-aided design-for-reliability tool for upfront evaluation of attachment reliability for both conventional and area-array Surface Mount (SM) assemblies. Large populations of SM products have been deployed in the last five to ten years with few known instances of solder joint fatigue failures in commercial and industrial applications. High-yields, rigorous process controls, small size components, CTE matching techniques and compliant lead attachment have all contributed to the successful and reliable implementation of SM assemblies. Military, avionics, aerospace, automotive, telecommunication and other applications with extended design lives or stringent reliability requirements have required careful consideration of solder reliability issues at the design stage. The reliability challenges brought about by new assembly technology are made even more difficult by the shortening of engineering cycles. With growing trends toward larger packages for higher I/O count, increasing power dissipation, low-profile IC packages with shorter leads and large silicon content, and an increasing use of leadless area-array packages, solder reliability issues have resurfaced that must be addressed at the design stage rather than as an after-thought. Modeling tools play an essential role in addressing these issues and in expediting the reliability assessment process.

## COMPONENT DESIGN AND ATTACHMENT RELIABILITY

Figure 1 shows the impact of component design on attachment reliability and gives a relative ranking of attachment reliability for several classes of SM components on organic boards. This ranking is not absolute since reliability is *application dependent* and design parameters vary within a family of packages. Nevertheless, the following trends are fairly well established:

- In general, LCCCs on organic boards have less attachment reliability because of solder creep-fatigue due to large cyclic strains and stresses in the solder joints under thermal cycling conditions [1, 2, 3]. Design parameters that may impede solder joint reliability are: low component stand-off, limited fillet size, large component size and the CTE mismatch between low expansivity LCCCs and high expansivity organic boards.
- Discrete components such as SM capacitors and resistors also have a ceramic type body. Because of their small size, large solder attach areas and fillets, their attachment reliability has not been a concern in most environments except perhaps for automotive under-the-hood applications [4].
- Plastic leaded packages with copper leadframes and tall compliant leads have the highest attachment reliability. This includes packages like Plastic Leaded Chip Carriers (PLCCs) and Plastic Quad Flat Packs (PQFPs). The compliant leads act as elastic springs that provide strain relief and absorb the in-plane thermal expansion mismatch between components and boards. With adequate compliance built-in, stresses transmitted to the solder joints are low and, in most cases, the resulting creep strains do not lead to much creep-fatigue damage. Several methods are available to characterize lead compliance and spring constants [5, 6].
- Plastic and ceramic packages with shorter leads and Alloy42 or Kovar type leadframes have less attachment reliability. With low profile Alloy42 Thin Small Outline Packages (TSOPs) [7], the global mismatch problem is exacerbated by the low expansivity of a component with high silicon content, and short, stiff leads that do not provide sufficient strain relief. Low expansivity leadframe materials (about 6 ppm/°C for Alloy42) also create a large local expansion mismatch between the lead foot and the high expansivity solder (about 24 ppm/°C for near-eutectic Sn-Pb). Whether this is detrimental needs to be assessed on a case by case basis.

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<sup>1</sup>LCCC = Leadless Ceramic Chip Carrier

<sup>2</sup>CTE = Coefficient of Thermal Expansion

- For BGA technology [8], reliable attachment and extended design lives can be achieved by optimizing package and joint design parameters [9-12] to decouple the stiff, low expansivity die from high expansivity organic boards. BGA attachment onto circuit boards is leadless as with LCCCs. However, package and board compliance, tall joints and large solder attach areas help reduce solder joint strains and stresses.

Attachment reliability (or the lack of it) for competing SM miniaturization technologies is not well established yet [13, 14] except perhaps for Lead-On-Chip (LOC) [15] and flip-chip with underfill [16-20]. Design-for-reliability and optimization techniques that have been validated for other package and assembly types are expected to apply to CSP assemblies as well. The PBGA model described in the latter part of this paper applies directly to area-array assemblies such as mini- and micro- BGAs.

## SOLDERED ASSEMBLY RELIABILITY MODELING

Solder joints fail in a wear-out mode with component assembly failure rates increasing over time. Reliability modeling is required for upfront prediction of attachment failure rates or to extrapolate failure distributions from accelerated life tests to field conditions. Modeling also is a cost effective way to optimize package and assembly parameters. The end goal is to ensure that failure rates at the end of the intended design life meet customers' reliability requirements.

Solder interconnect reliability modeling has been the subject of intensive studies for over 25 years [1, 21, 22]. Predicting solder joint fatigue life and assembly failure rates is a difficult problem because of the complex mechanical behavior of solder, the three-dimensional (3D) structure of real electronic assemblies and the statistical nature of fatigue failures. A 1995 review of several solder reliability models is given in [23, 24]. All models have their own merit and trade-offs between different approaches are in terms of accuracy, applicability, validity, cost, availability, ease of use and skills required. Here, models are grouped into four categories based on the computational resources needed to run them:

- *Calculator models.* These technology-specific models include temperature and frequency effects [1, 22]. Local mismatch is not included since global mismatch had a dominant effect in the assemblies these models were developed for. One example of a calculator model is the Norris-Landzberg (NL) model [22] which was developed for bare die flip-chip assemblies on ceramic substrates. The reliability of flip-chip solder joints, as supported by the NL model, has been proven by over 30 years of use in mainframe applications [25]. Recent data [9] suggests that the NL model may also apply to ceramic area-array assemblies on organic boards.
- *PC-based models.* Two examples of PC-based models are the Comprehensive Surface Mount Reliability (CSMR) model [26, 27] and the SRS model -- the latter model is presented in the next section of this paper. Both include plastic flow and creep of solder, as well as local CTE mismatches and failure statistics. Structural analysis is one-dimensional. The correlation of accelerated test data uses inelastic strain energy as a measure of cyclic damage. The CSMR and SRS models have been validated over a wide range of components and near-eutectic Sn-Pb assembly technologies.
- *Workstation models.* Two examples of models that are run on workstations are the Motorola model [28, 29] and Ford's CAIR system [30]. Workstation power is needed for 3D non-linear, temperature and time-dependent Finite Element Analysis (FEA) in the Motorola model and others. Solder joint life is predicted using strain energy based statistical crack initiation and crack growth models that have been validated over a wide range of components and assembly technologies. In spite of some differences in the core of the Motorola and the above PC-based models, life predictions and trends derived from either model are similar.
- *Supercomputer models.* 3D models intended to capture the intricate details of solder micro-structural evolution, crack initiation and crack growth have been developed [31, 32]. Specialized FEA codes are used and the size and complexity of the models requires super-computer resources.

Many model development efforts are underway in industry and universities. The examples above do not constitute an exhaustive list and the reader is referred to [23, 24] for a more extensive review. PC-based and workstation models that have been validated for a wide range of technologies appear well suited for engineering applications.

## SRS MODEL

The Solder Reliability Solutions (SRS) model builds upon the CSMR methodology [26, 27]. The reader is referred to [26, 27] for background information on the CSMR model. Innovative features of SRS are:

- Bending of parts is included for leadless component attachment. This effect is important for leadless area-array plastic packages and CSPs where the component flexural compliance, which depends on the package contents and construction, provides for significant stress and strain relief in the solder joints.
- Inelastic strain energy is from complete hysteresis loops with different dwell times on the hot and cold sides of thermal cycles.

- The local mismatch stress/strain response is determined from the combined and simultaneous action of solder/board and solder/lead (or component) CTE and modulus mismatches. The analysis uses a tri-layer model which also accounts for the local effects of board to lead (or component) CTE and modulus mismatches.
- Fatigue life from component test vehicles is correlated on a joint per joint basis. For peripheral I/O components, all joints are treated as equal to the worst case “corner” joints.

More details on the mechanics of SRS are given in [33]. The fatigue life correlation in Figure 2 gives joint characteristic lives scaled for the solder crack area versus cyclic inelastic strain energy:

$$\alpha_{\text{joint}} / A = C * (6.149 \times 10^7) / \Delta W^{0.998}$$

where  $\alpha_{\text{joint}}$  is the joint characteristic life or cycles to 63.2% failures in the joint population, A is the solder crack area,  $\Delta W$  is the inelastic strain energy per cycle (sum of strain energies due to global and local mismatches) and C is a calibration factor. C equals 0.434 for the lower bound of the correlation band in Figure 2, 1 for the centerline and 2.7 for the upper bound. The correlation in Figure 2 is from 19 accelerated tests of leadless and leaded assemblies. The least squares goodness-of-fit correlation coefficient for the data in Figure 2 is 0.965. Scatter is 2.3 times below the centerline and 2.7 times above, which is typical of fatigue data and of similar amplitude as in other models [26-29]. The model was frozen as shown in Figure 2 and the correlation was later validated with failure data from five PBGA accelerated tests [11] and experimental trends from PBGA parametric studies [11, 12, 29] (see PBGA section). That is, the correlation is supported by over 24 experiments. The slope of the life data correlation is about -1, close to those of CSMR [26, 27] and R. Darveaux’s crack growth model [28, 29]. Also shown in Figure 2 is a straight line of inverted mean propagation rates (“dA/dN”) from R. Darveaux’s crack propagation model [28]. Since the difference between mean and characteristic lives is small, the fit of Darveaux’s crack growth rate to the average crack propagation rates of SRS is good. The two models are consistent and validate one another.

One limitation of the present version of SRS is that temperature ramp-rates are not included in the stress/strain analysis. This is not a concern, in general, except for applications with very slow ramps or very short dwells. Ramp-rates in the tests that were used to establish the SRS correlation were typical of single or double chamber air-to-air thermal cycling -- in the range 5 to 80°C/min -- and this did not seem to have an effect on the correlation. By not including creep during the temperature ramps, the analysis underestimates the initial inelastic deformations but this leads to higher stresses building up, which in turn leads to larger creep rates and strains during the dwell periods. This is thought to be conservative for making reliability predictions because the resulting stress/strain hysteresis loop has, in general, a larger area than when creep is included during the ramps. Ramp-rates will be included in future refinements of SRS.

A list of eighteen input parameters used in SRS and a table of thermal conditions for accelerated testing or multiple thermal loads in the field are given in Appendix. Additional parameters and component mechanical drawings are needed for lead stiffness calculations and PBGA analysis. Detailed geometric data is also required to construct FEA models. Handbook values can be used for standard material properties (e.g.: silicon). Measurements are needed for product specific materials and constructions (e.g. in-plane expansivities of organic boards or component CTEs). This makes data gathering a significant part of the reliability evaluation process. Model development and validation have suffered from a lack of standard formatting of test vehicle information and accelerated test data is reported with varying degrees of completeness. Sometimes, test information and material properties are available by direct communication with the authors and material suppliers. In other cases, the information is unavailable because of the purpose of the experiment (e.g.: A to B comparison testing) or the proprietary nature of the data.

## PLASTIC BALL GRID ARRAYS

The reliability of area-array assemblies has received considerable attention [9-12, 28, 29, 34-41]. Design parameters with the greatest impact on PBGA assembly reliability are: pad diameter, laminate thickness, die size and thickness, and solder joint height. In general, there is little effect of normal assembly processes, board finish [12], solder paste or flux [40]. Assembly repair may have a negative or positive impact on fatigue life (less than  $\pm 20\%$  from the data in [12]). Defective joints due to process degradation, such as “double reflow” overstress [41], are candidates for infant mortality failures but they can be avoided by adjusting process parameters. Good wetting and quality solder joints are necessary and design-for-reliability is an important step in the implementation of reliable area-array technology in various product environments.

The application of SRS to PBGA assemblies is presented below where a procedure is outlined to determine effective CTE and assembly stiffness parameters for input to the reliability model. Since the two rows of joints near the edge of the die are the most susceptible to failure [10-12] when global mismatch is large, the effective CTE and stiffness parameters are estimated at the edge of the die. Existing approximate solutions for thermal stress analysis of multi-layered structures and composite plate mechanics are used and are justified a-posteriori by comparing predicted versus experimental fatigue life for several PBGA constructions and assembly parameters. The effective component CTE under and at the edge of the die is obtained by thermal stress analysis of a multi-layer axisymmetric stack [42]. A schematic of the PBGA multi-layer stack in the die area is shown in Figure 3. The stack has 7 layers. It was found that it is important to include solder mask in the analysis. Material properties that are required for each layer are: CTE, Young's modulus and Poisson's ratio. With thickness parameters, the total input is: 7 layers x 4 parameters each = 28 parameters to determine the effective CTE of the PBGA under the die. From thermal stress analysis, we obtain the effective CTE as:  $CTE_{eff}(PBGA) = \epsilon_x(\text{bottom}) / \Delta T$  where  $\epsilon_x(\text{bottom})$  is the normal strain (mechanical + thermal) at the bottom of the PBGA stack subject to a temperature swing  $\Delta T$ . This effective CTE is a measure of the in-plane free thermal expansion at the bottom of the PBGA construction and represents the component CTE seen by the solder joints under the die due to in-plane thermal expansion mismatch between the component and the motherboard.

The assembly stiffness of a leadless assembly includes spring constants for stretching and bending of boards and components [43-45]. Bi-metallic strip bending provides most of the compliance of LCCC assemblies and Moiré field displacements have shown that bending also is a significant deformation mode for area array assemblies [12, 38, 46]. From strength of materials and plate theory [47], the equivalent bending and stretching rigidities of the PBGA multi-layer construction are:  $D = \sum D_i$  and  $S = \sum S_i$ , where  $D_i = E_i h_i^3 / [12 (1 - \nu_i)]$  is the plate rigidity of the  $i^{th}$  layer in flexure and  $S_i = E_i h_i / (1 - \nu_i)$  is the stiffness of the  $i^{th}$  layer in tension.  $E_i$  and  $\nu_i$  are Young's modulus and Poisson's ratio for the  $i^{th}$  layer material;  $h_i$  is the thickness of the  $i^{th}$  layer. The PBGA composite rigidities are then used to derive equivalent Young's moduli for tension and flexure of an equivalent, homogeneous component of thickness  $h_C$  equal to the total thickness of the PBGA package. A simple rule of mixtures is used to define the PBGA equivalent Poisson's ratio [48]. The properties of the equivalent package are then fed into a leadless assembly stiffness model [43-45].

#### Model Validation

The PBGA analysis and reliability model are validated against five 225 I/O PBGA datasets and parametric analysis from Motorola's design-of-experiments [11]. The package and assembly variables and accelerated test results for the five datasets are summarized in Table 1 where dataset A is the reference configuration. The two-parameter (2P) Weibull characteristic life and slope for dataset E were updated from the original Motorola publication [11], with more accumulated test cycles providing for more accurate parameter estimates [49]. The reported characteristic lives were on a per component basis. Geometry, material properties and test conditions are from [11, 34-36, 50].

| <i>Dataset</i> | <i>Characteristic life<br/>a (cycles)</i> | <i>2P Weibull<br/>slope b</i> | <i>Variables</i>   |
|----------------|---|-------------------------------|--|
| A              | 7958                                      | 13.0                          | None (reference package and assembly).   |
| B              | 6851                                      | 11.2                          | Lower stand-off: 20.8 mil vs. 22.2 mil due to non-solder mask defined (NSMD) pads on test board.   |
| C              | 10292                                     | 9.92                          | Thinner die: 0.36 mm (14.2 mil) vs. 0.45 mm (17.7 mil)   |
| D              | 12269                                     | 12.7                          | Low modulus die attach and thinner die (0.36 mm vs. 0.45 mm)   |
| E              | 14446                                     | 11.3                          | Thick PBGA substrate: 0.76 mm (29.9 mil) vs. 0.36 mm (14.2 mil) and lower stand-off: 19.6 mil vs. 22.2 mil due to NSMD pads on the test board. |

**Table 1:** Motorola's 225 I/O PBGA design-of-experiments and accelerated test results [11, 49].

Cyclic inelastic strain energies were calculated for each test vehicle. The data is shown in Figure 4 where the test characteristic lives, which were on a per component basis, were converted to a per joint basis using a 2P Weibull scaling factor of  $n^{1/\beta}$  times where  $n$  is the number of susceptible joints per component. That is, the component assembly reliability is determined by a subset of worst case joints in the rows near the edge of the die. The 2P Weibull scaling factor represents a shift in the component and joint failure distributions on Weibull paper. Also, to be on the conservative side, all joints are considered to fail as the highly stressed “corner” joints at the edge of the die and in the diagonal direction of the package. We take  $n = 24$  for the row of 24 joints under the edge of the die. The component to joint conversion factor then is:  $n^{1/\beta} = 1.07$  to  $1.38$  for the values of  $\beta$  in Table 1. For  $n = 56$ , the conversion factors are slightly higher:  $n^{1/\beta} = 1.08$  to  $1.50$ . Thus, working with the inner net of 24 joints is more conservative for converting component characteristic lives to worst joint characteristic lives. As seen in Figure 4, the Motorola test results fit the SRS correlation band well. Figure 5 shows test characteristic lives on a component basis versus predicted lives on a per joint basis and on a net basis, with nets of 24 or 56 joints. In all cases, the data fits the model within a factor of two times, which is better than typical for fatigue. Life predictions on a per joint basis appear to give the best fit. The predicted trends for dataset A versus datasets B, C and E agree with experimental results, that is, the model captures the effect of changes in joint height (A vs. B), die thickness (A vs. C) and PBGA substrate thickness (A vs. E).

The effect of low modulus versus standard die attach material is not as clear cut. For dataset D, the PBGA had both a thinner die and low modulus die attach and those two effects are confounded in the test results. SRS predicts that, for a standard die thickness (dataset A), a change from standard die attach epoxy to low modulus epoxy with high CTE is slightly detrimental to assembly reliability. Others [40] also report that low modulus die attach did not always provide the expected reliability improvements, with a 1.31 times negative effect on fatigue life or a possible improvement of 1.45 times [40]. Sample sizes were small (9 to 13 components) and the data may have too much scatter for a definite resolution of die attach effects. Possible explanations of the discrepancy between our predicted trends and test results for A vs. D are: 1) the high expansivity of low modulus epoxies (CTE > 200 ppm/°C vs. 2.8 ppm/°C for silicon) may have led to die attach delamination failures that would make for a more compliant PBGA package; 2) the die attach effect in the experiment may have been overshadowed by the die thickness effect; 3) the PBGA analysis, based on tensile and flexural stresses in a multi-layer stack, does not account for shear stresses at material interfaces, and this effect may be important for low modulus die attachment.

Datasets A and B also provide for a direct comparison of assemblies with SMD and NSMD pads on the test boards. The stand-off heights were 22.2 mils and 20.8 mils, respectively. “Stress raiser” or “stress concentration” effects have been advocated [12, 37] to explain differences between assemblies with SMD or NSMD pads. The slightly different shapes of the two joint types are not accounted for in the SRS analysis and there is no attempt to include stress concentration factors because they apply only to linear elastic structures [47, 51, 52]. Nevertheless, SRS predicts the experimental trends for NSMD versus SMD pads based on height differences alone. In this particular design, the height dependence appears to overshadow solder mask driven stresses and other stress raiser effects.

#### Parametric Studies and Experimental Results

The SRS reliability model is further validated by parametric studies on pad diameter, stand-off height and PBGA substrate thickness. Predictions are compared to published test results and trends obtained by FEA modeling.

##### *Effect of Pad Diameter*

The pad diameter for the standard 225 I/O PBGA assembly was 24 mil (dataset A). Here, the pad diameter is varied in the range 18 to 30 mil. Results are shown in Figure 6. The trends shown in Figure 6 are for specific test vehicle (dataset A) and accelerated test conditions [11] and they are expected to vary for other assemblies and thermal conditions. The SRS predictions are from the centerline of the model correlation band, scaled for the characteristic life of dataset A. The SRS trend is similar to that obtained by R. Darveaux et al. [11] using FEA modeling. On the SRS curve, we have included pad diameters of 0.64 mm (25.2 mil) and 0.76 mm (29.9 mil) for which accelerated test results were reported by AT&T in [12]. The ratio of predicted fatigue lives for the latter two diameters is: 1.79, close to an average ratio of 1.7 from experimental trends in [12]. One possible source of discrepancy is that we used the 225 I/O PBGA assembly parameters from dataset A since all the necessary material properties, solder volume and design parameters are not given in [12]. Nevertheless, the general agreement between SRS, FEA modeling and experimental results is good and the two modeling approaches capture pad diameter effects well. Increasing the pad solderable area is doubly beneficial since the enlarged load bearing area decreases stress levels and the larger solder crack area provides for longer crack propagation times.

### *Effect of Stand-off Height*

The stand-off height for the standard 225 I/O PBGA assembly was 22.2 mil (dataset A). Here, the solder joint height is varied in the range 17 to 30 mil. Results of the SRS model are shown in Figure 7. Design curves like the one in Figure 7 are of use in assembly coplanarity studies. For example, for a nominal height of 22.2 mil (dataset A), Figure 14 suggests that a  $\pm 2$  mil variation on height has an impact of less than  $\pm 10\%$  on fatigue life. A  $\pm 4$  mil variation has an impact of  $\pm 15\%$ .

Stand-off heights of 20.5 and 29.3 mils are shown in Figure 7, for which the predicted life improvement is 28%. This is close to the 27% improvement reported by R. Darveaux et al. [11] for those two solder joint heights, although the experimental data was for a 72 I/O PBGA assembly [29] and the thermal cycle had a larger temperature swing (-40 to 125°C) which, perhaps, compensates for size differences. The experimental and predicted life improvement is less than a 100% improvement given by calculator models. The FEA modeling procedure used in [11] gives a conservative 4% improvement. As discussed in [11], post-processing of FEA results using maximum strain energy values in the solder joints can overestimate local mismatch effects because of mesh size sensitivity and strain energy singularities. In a more recent study, R. Darveaux [53] found that mesh sensitivity can be reduced by averaging strain energies across element layers near the critical interfaces. The life-to-height dependence predicted by FEA modeling then is similar to the one in Figure 7. While empirical, the averaging process that is required to smooth out FEA results appears to work well.

In this study of stand-off height effects, SRS gives local mismatch contributions (percent of total cyclic inelastic strain energy) of 46, 56 and 70% for heights of 17, 22.2 and 30 mil, respectively. This is consistent with a 67% fatigue life improvement predicted by FEA modeling for a stand-off height of 22.2 mil, and using a CTE of 15 ppm/°C for solder [11] to minimize local mismatch effects. Even though the 225 I/O PBGA was mounted on a board with a large in-plane CTE (about 17.6 ppm/°C), the package and assembly design parameters provide significant global CTE mismatch relief and local mismatch is a large contributor to the solder joint cyclic strain energy. This effect is confirmed by both SRS and FEA modeling [11]. The importance of local mismatch for PBGA assemblies has also been demonstrated experimentally. Moiré results reported in [38] show that, in a “Shell/Gel” PBGA type assembly where the silicon tile is largely decoupled from the PBGA laminate by design, bending due to global mismatch is small and strains in the solder joints are due mostly to local mismatch.

### *Effect of PBGA Substrate Thickness*

The PBGA substrate thickness for the standard 225 I/O PBGA assembly was 0.36 mm (datasets A, B) including solder mask on top and bottom. Here, the total thickness of the substrate changes from 0.36 mm (14.2 mil) to 0.76 mm (29.9 mil). Results from SRS, FEA modeling [39] and accelerated testing [39] are shown in Figure 8. The SRS predictions were scaled for the characteristic life of dataset B. The trends are close and the relative fatigue lives for the 0.76 mm vs. 0.36 mm substrate agree with the 2.1 times improvement in accelerated testing (dataset B versus E). Improvements of similar amplitude have been reported in [12] although a more accurate, quantitative comparison is not possible because the necessary material properties and design parameters are not available.

From SRS and PBGA stress analysis, the relative life improvement is attributed to a 32% increase in the PBGA effective CTE and a 13% decrease in assembly stiffness both of which reduce the strain energy due to global mismatch. The assembly stiffness decreases because it gets more contribution from the low modulus core of the PBGA substrate than from the high modulus silicon die. Figure 9 shows the contributions of local and global mismatches to the total cyclic strain energy versus substrate thickness. The global mismatch strain energy decreases with increasing substrate thickness while the local mismatch strain energy stays almost constant, as expected. The latter decreases slightly because the impact of low expansivity silicon on local mismatch also decreases with thicker substrates. When the substrate thickness increases from 0.36 to 0.76 mm, the relative contribution of local mismatch to the total strain energy increases from 56 to 98 %. That is, global mismatch becomes insignificant and the 0.76 mm thick substrate effectively decouples the silicon die from the motherboard.

## ACCELERATED LIFE TESTING

In this section, SRS is used to assess the efficiency of accelerated thermal cycling tests. Table 2 gives test profile parameters for eight conditions, A to H. The parameters are from a quick, non-inclusive survey of test profiles in post-1992 publications. Cyclic frequencies are 6 to 144 cycles/day with dwell times as short as 1 minute in a 10 minute cycle (condition B) or as long as 30 to 50 minutes in a 4 hour cycle (condition H). The smallest temperature swing is 80°C, the largest one 180°C. An “average” test condition is defined by averaging across conditions A to H.

| <i>Test Condition</i> | <i>T<sub>cold</sub></i> | <i>T<sub>hot</sub></i> | <i>Frequency</i> | <i>Cycle Length</i> | <i>Dwell Times</i>       |                         | <i>Ramp rates</i>        |
|-----------------------|-------------------------|------------------------|------------------|---------------------|--------------------------|-------------------------|--------------------------|
|                       | (°C)                    | (°C)                   | (cycles/day)     | (minutes)           | <i>Cold</i><br>(minutes) | <i>Hot</i><br>(minutes) | (up or down)<br>(°C/min) |
| A                     | 0                       | 100                    | 48-96            | 15-30               | 5                        | 5                       | 10-40                    |
| B                     | -10                     | 110                    | 144              | 10                  | 1                        | 1                       | 30                       |
| C                     | 15                      | 100                    | 33               | 44                  | 5                        | 5                       | 5                        |
| D                     | -10                     | 70                     | 144              | 10                  | 1                        | 1                       | 20                       |
| E                     | -55                     | 125                    | 55               | 26                  | 12                       | 12                      | 180                      |
| F                     | -40                     | 125                    | 24               | 60                  | 15                       | 10                      | 9.5                      |
| G                     | 0                       | 100                    | 72               | 20                  | 4-6                      | 4-6                     | 16                       |
| H                     | -55                     | 100                    | 6                | 240                 | 30-50                    | 30-50                   | 2                        |
| "AVERAGE"             | -19                     | 104                    | 69-77            | 21-30               | 6-8                      | 6-8                     | 16-35                    |

**Table 2:** Survey of test conditions.

Test efficiency is defined as damage or inelastic strain energy per unit of time. Results are shown in Figures 10 and 11 for a LCCC type test vehicle (TV1) and an Alloy42 TSOP test vehicle (TV2), respectively. A FR-4 type substrate was used in the analysis. Test efficiency is highest for conditions B and E and is about twice as large as for the “average” test condition. These trends hold for the two test vehicles, TV1 and TV2, although there are slight differences between Figures 10 and 11, similar to acceleration factors being component dependent. What makes conditions B and E more efficient is that B has the shortest dwell times (1 minute) and E has the largest temperature swing and fastest ramps. Although other considerations come into play when selecting thermal profile parameters for accelerated testing [45], the analysis above suggests that there is room to improve test efficiency.

The effects of variable dwell times on fatigue life for a 0-100°C cycle and the standard 225 I/O PBGA test vehicle are shown in Figures 12 and 13. Figure 12 gives the effect of equal cold and hot dwells as predicted by SRS, Motorola's one dimensional (1D) models (using Darveaux's and Anand's constitutive equations for solder) and FEA [11]. Results from the three 1D models are in good agreement. The discrepancy with FEA results is not well understood and is perhaps related to the sensitivity of FEA solutions to element size and time steps. In Figure 13, the SRS analysis was repeated with a constant 5 minute dwell on one side and a variable dwell time on the opposite side of the thermal profile. The results show that, due to rapid stress relaxation at 100°C, there is little effect of increasing the dwell time on the hot side of the cycle. Most of the reduction in fatigue life is attributed to increased creep strains at 0°C when the duration of the cold dwell is increased.

## CONCLUSIONS

A solder interconnect reliability model has been developed and validated for a wide range of SM technologies, including PBGAs. The PBGA type of analysis applies directly to area-array CSP assemblies. The model has been implemented as a PC-based design-for-reliability tool. While knowledge of component, board and assembly design parameters is needed for data input and interpretation of the results, the model does not require any special numerical or computational skills, and it is intended to provide for rapid solder joint reliability assessment at the product design stage or in day-to-day engineering applications. Model refinement is in progress, including validation for more recent miniaturization assembly technologies and extension to more complex thermal conditions.

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## APPENDIX: MODEL INPUT PARAMETERS

Input parameters for reliability evaluation using SRS and assembly stiffness models are listed below. Component mechanical drawings, solder joint cross-sections are essential information as well. Lead geometry and material properties are also needed for leaded assemblies stiffness calculations. Also needed for PBGA analysis are the material properties and thickness of internal layers, plus pad thickness and properties for the laminate copper pads.

- Component Data:
  - ◇ Distance to Neutral Point (in)
  - ◇ Component thickness (in)
  - ◇ Effective in-plane component CTE (/C)
  - ◇ Effective Young's modulus in tension (psi) (for global mismatch)

- ◇ Effective Young's modulus in flexure (psi) (for global mismatch)
- ◇ Thickness of lead or component at solder joint (in)
- ◇ Effective CTE of lead or component at solder joint (/C) (for local mismatch)
- ◇ Effective Young's modulus of lead material or component (psi) (for local mismatch)
- Substrate Data:
  - ◇ Effective in-plane CTE in diagonal direction of component (/C) (determined from X and Y in-plane CTEs and component aspect ratio)
  - ◇ Effective Young's modulus (psi) in tension
  - ◇ Effective Young's modulus (psi) in flexure
  - ◇ Thickness
- Assembly Data:
  - ◇ Assembly stiffness (lb/in) (diagonal lead stiffness for leaded assemblies or combined stretching and bending stiffness of parts for leadless assemblies)
  - ◇ Solder joint effective thickness, component stand-off (in) (half the solder paste thickness for leaded assemblies)
  - ◇ Solder joint load bearing area / crack area (in<sup>2</sup>)
- Reliability Parameters:
  - ◇ Number of susceptible I/Os
  - ◇ Slope of 2P Weibull distribution
  - ◇ Intended design life (years)
- Thermal Conditions (typical of worst case product environment):

|             | <i>Hot Temp.</i><br>(°C) | <i>Cold Temp.</i><br>(°C) | <i>Hot Dwell</i><br>(minutes) | <i>Cold Dwell</i><br>(minutes) | <i>Fixed Cycle</i><br>Count<br>(cycles) | <i>Frequency of</i><br>variable cycles<br>(cycles/day) |
|-------------|--------------------------|---------------------------|-------------------------------|--------------------------------|---|--|
| Condition 1 |                          |                           |                               |                                |   |  |
| Condition 2 |                          |                           |                               |                                |   |  |
| Condition 3 |                          |                           |                               |                                |   |  |
| Condition 4 |                          |                           |                               |                                |   |  |
| etc...      |                          |                           |                               |                                |   |  |

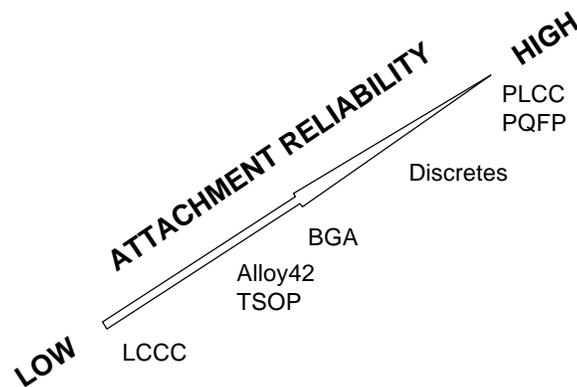
*Note:* Fixed cycles occur at the beginning of the product life cycle (e.g.: EST, shipping, storage...). Variable cycles occur throughout the product life at an estimated frequency in cycles/day (e.g.: season-dependent environmental cycles for outdoor equipment; usage cycles: on/off cycles, mini-cycles, etc...).

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**Fig. 1:** Attachment reliability of SM components on organic circuit boards.

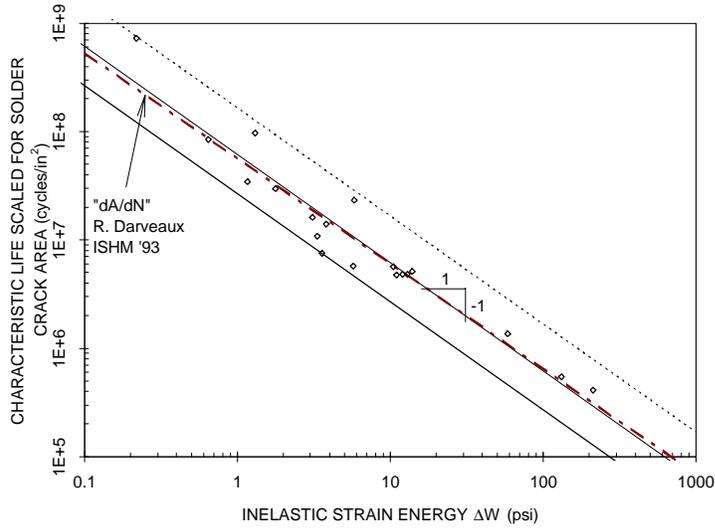


Fig. 2: SRS correlation of accelerated test data.



Fig. 3: Schematic of multi-layer model used in PBGA analysis.

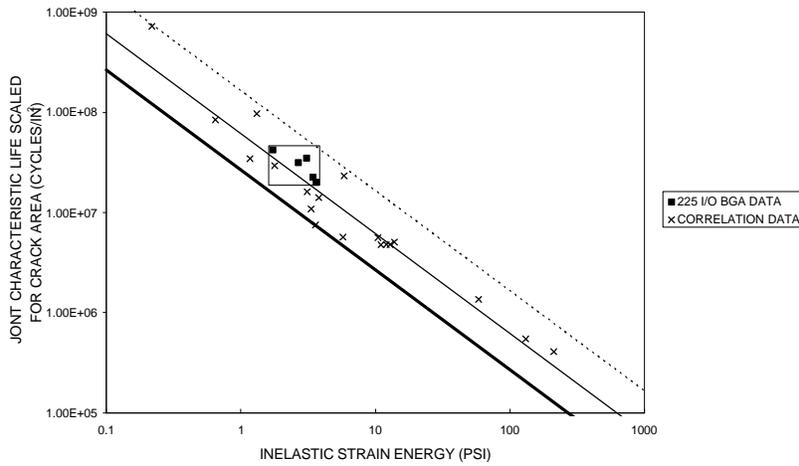


Fig. 4: Fit of Motorola's 225 I/O PBGA data [11, 49] to the SRS correlation band.

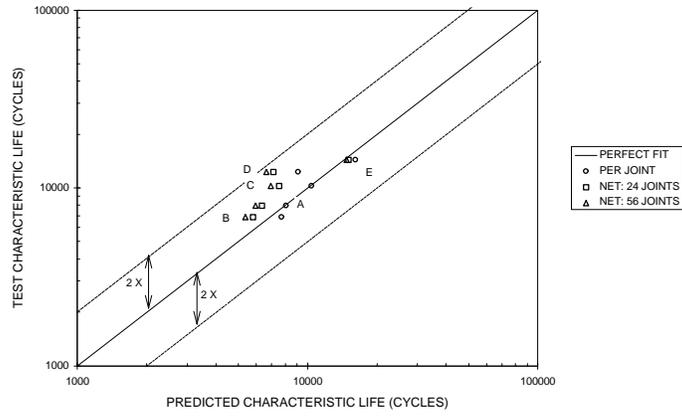


Fig. 5: Measured vs. predicted lives for 225 I/O PBGAs. Labels refer to datasets A-E in Motorola's tests [11, 49].

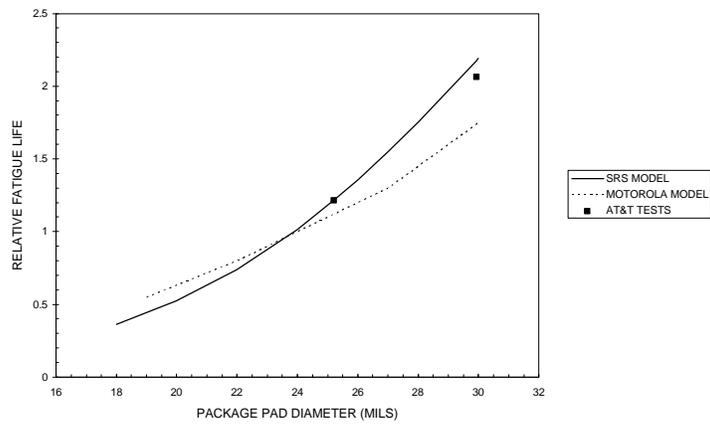


Fig. 6: Effect of package pad diameter on fatigue life.

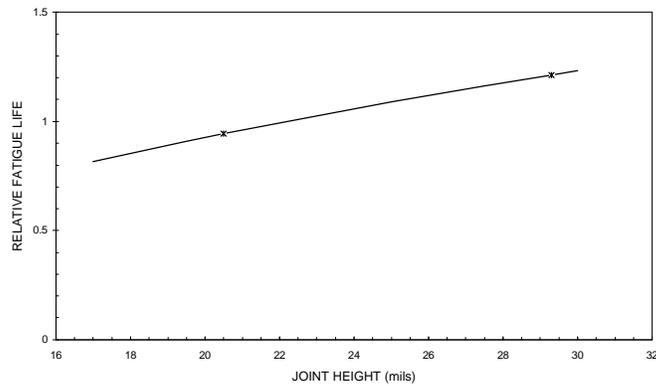


Fig. 7: Effect of stand-off height on fatigue life (SRS predictions).

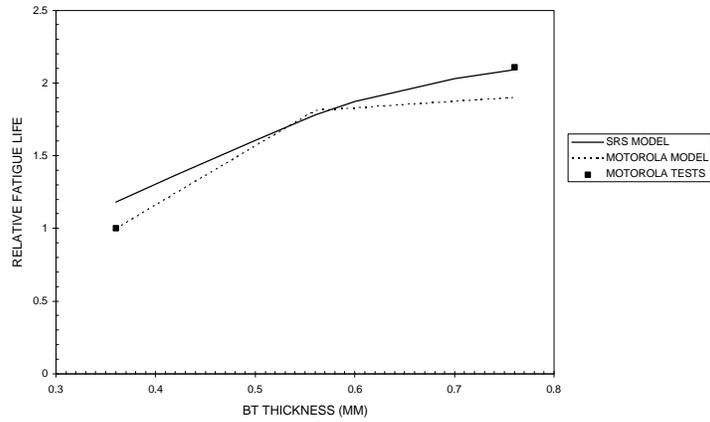


Fig. 8: Effect of PBGA substrate thickness on fatigue life.

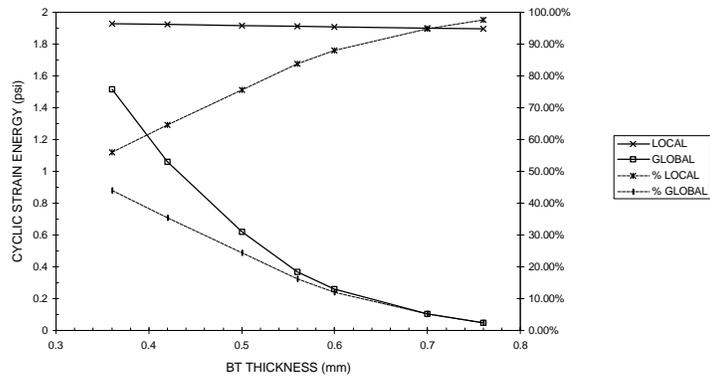


Fig. 9: Local and global strain energy contributions as a function of PBGA substrate thickness.

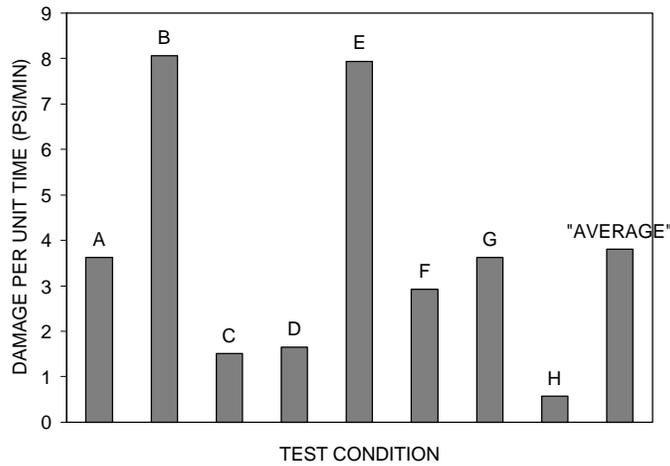


Fig. 10: TV1 (LCCC): Inelastic strain energy per unit of time for various test conditions.

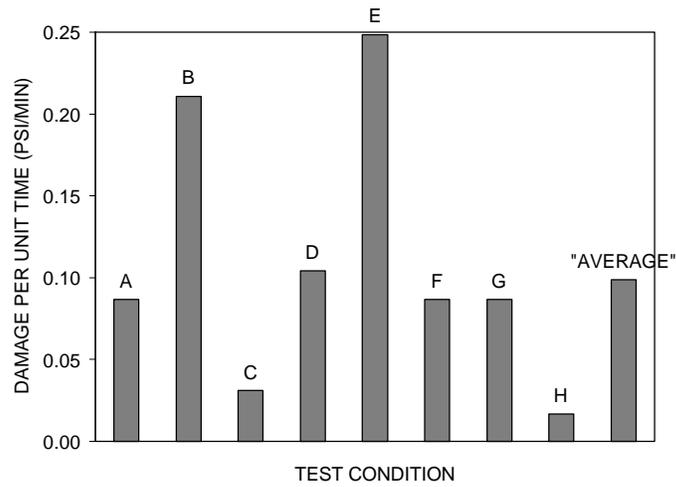


Fig. 11: TV2 (Alloy42 TSOP): Inelastic strain energy per unit of time for various test conditions.

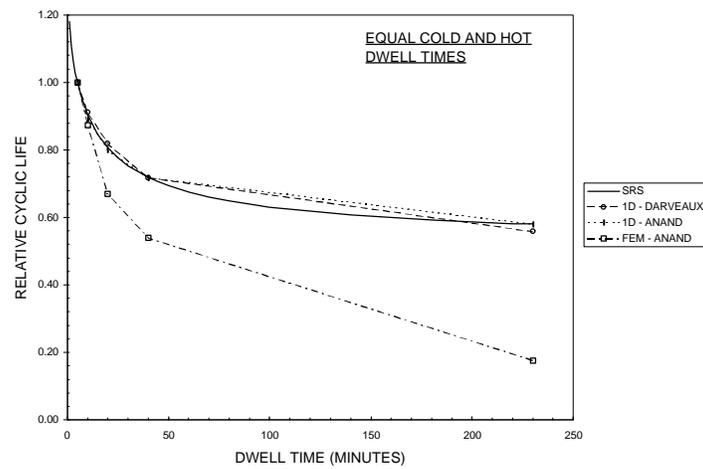


Fig. 12: Effect of dwell time on fatigue life for equal cold and hot dwells; comparison of 1D and FEA results.

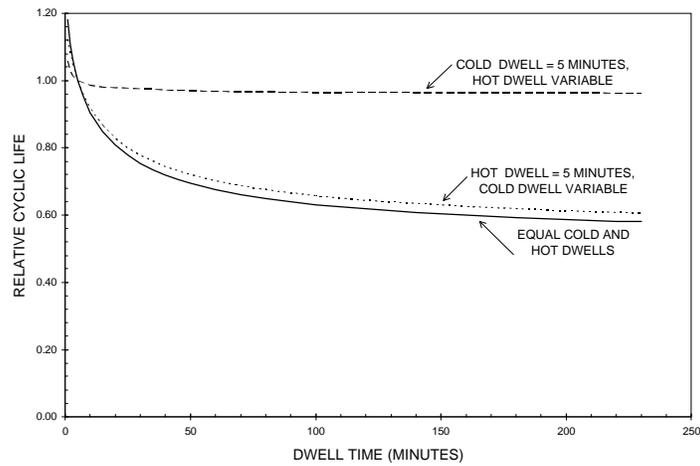


Fig. 13: Separate effects of variable cold and/or hot dwell times on fatigue life.