

SOLDER JOINT RELIABILITY OF CSP VERSUS BGA ASSEMBLIES

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NOTE: This paper covers validation of the SRS model for a variety of BGA, flip-chip and CSP assemblies.

1. Introduction

A general trend of Flip-Chip (FC) and Chip Scale Package (CSP) assemblies is that their solder joints tend to fail earlier than those of their BGA or QFP counterparts under thermal cycling conditions. Solder interconnects remain the weakest link of modern Surface Mount (SM) assemblies. Safety margins have been reduced and the extrapolation of test failure data to field conditions calls for more accurate life prediction techniques than the simplified algebraic models that were used in the past.

This paper documents on-going efforts to validate the Solder Reliability Solutions (SRS) model for flip-chip, CSP and BGA assemblies. The analysis shows that the attachment reliability of each package type can be interpreted in terms of package construction, material properties and design parameters. Accurate characterization of package and board material properties is thus critical to establishing the attachment reliability of emerging packaging technologies.

2. Reliability Issues

Conventional SMT has proven to be reliable although some components have limited reliability (e.g., large leadless ceramic components or some low-profile leaded packages). While BGAs are leadless and often large, their saving grace has been the large volume of BGA solder balls and the high standoff of BGA components (typically 20 to 25 mils). Safety margins have been reduced for emerging technologies. The main factors that limit the reliability of CSP assemblies are their high silicon contents, the reduced size of CSP pads and the shrinking size of CSP solder joints. Related and on-going technical issues include the following:

- A lack of standardization for accelerated testing: while the need for standards is arguable, a set of standard test conditions and requirements would provide a common language to assess the reliability of circuit board assemblies. Such standards are currently being developed by an IPC task force.
- Difficulties in acquiring or reluctance to measure material properties for boards and components. E.g., measuring the in-plane CTE of circuit board is critical since the board thermal expansion is very much dependent on the laminate, copper contents and board features such as holes, vias etc... For FR-4 circuit boards, CTEs have been measured in the range 12 to 24 ppm/°C, that is, far beyond the often-quoted handbook values of 16 or 18 ppm/°C.

The above issues are being compounded with the advent of lead-free solders. The time frame to establish the reliability of packaging technologies, with consistency of data across the industry, has been of the order of five years. E.g., PBGAs were introduced in volume production around 1992. The intricacies of PBGA assembly reliability were worked out in the period 1992 to 1997 (e.g. Darveaux, 1995-97; Ejim et al., 1995-97). Similar time frames can be expected before the reliability of lead-free soldered assemblies is firmly established.

3. SRS Model

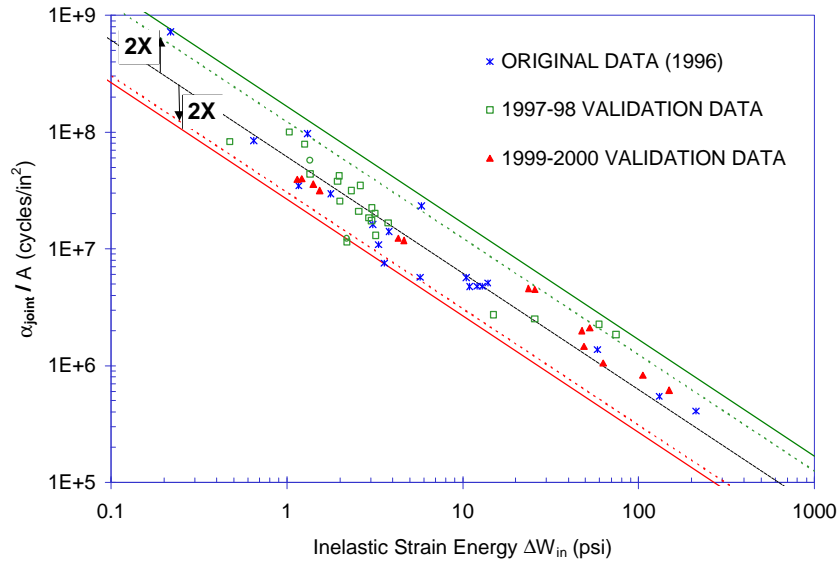


Figure 1: SRS correlation of SMT solder joint fatigue data.

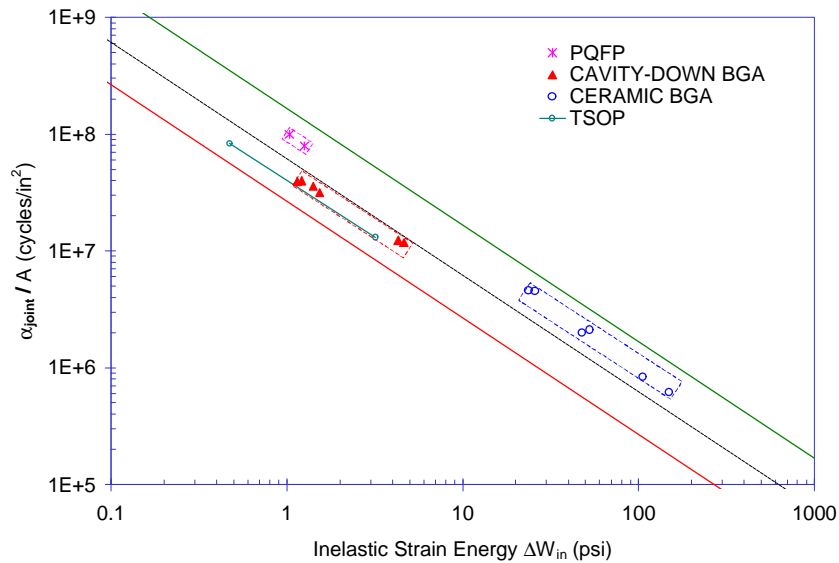


Figure 2: Fit of component-specific failure data to the SRS correlation band.

The SRS model is a life prediction model (Clech, 1996) that has been used since 1996. Given the semi-analytical, semi-empirical nature of the model, it is important to validate it for every new type of package. Validation data is presented below and in later sections of this paper. The model uses a strain-energy based fatigue law that was developed by correlating SMT fatigue data from 19 experiments. The original data is shown as stars in Figure 1 where the horizontal axis is the cyclic inelastic strain energy, ΔW_{in} , that is imparted to the solder joints and the vertical axis is the solder joint characteristic life, α_{joint} , scaled for the solder cracked area, A . Inelastic strain energy is obtained as the area of solder joint stress/strain loops during thermal cycling. The solder constitutive model includes temperature-dependent creep and plastic flow. The reader is referred to past publications (Clech, 1996/98) for further information on the mechanics of the model. The original correlation, with a slope of -1, was frozen as the best-fit line through those 19 data points (dashed centerline in Figure 1). The model has since been validated using failure data from over 35 experiments. The validation data is shown as squares (1997/98 data) and triangles (1999-2000 data) in Figure 1. The maximum spread of the data around

the model centerline is a factor 2.3 X below and 2.7 X above, which is typical of fatigue correlations. Most of the data (47 of the 54 data points) falls within a 2 X band shown in Figure 1. The model has also been validated for castellated LCCCs (Reichelt et al., 1999). A few data points from Figure 1 are highlighted in Figure 2:

- A set of 256 I/O PQFP assemblies under conditions: -40°C to 125°C and -55°C to 125°C (data after Lau et al., 1994, and Yeo et al., 1996).
- A set of 32 I/O Alloy 42 and Copper TSOPs under 0°C to 100°C conditions (data after Noctor et al., 1993).
- Six data points for three types of cavity-down BGAs (352, 540 and 560 I/Os) under conditions 0°C to 100°C and -55°C to 125°C (data after Ejim et al., 1997 and Ghaffarian, 1997-99).
- Six data points for CBGAs of three sizes (21 to 32 mm square) under two test conditions: 0°C to 100°C and -40°C to 125°C (data after Cho et al., 1996/98).

To a first order, rectangular boxes around each dataset are almost parallel to the model centerline. This suggests consistency of the data within each dataset and provides added confidence in using the model to derive acceleration factors.

4. PBGA Data and Pad Size Effects

| BALL DIAMETER | PAD DIAMETER (MM) | | JOINT HEIGHT (MIL) (predicted) | FATIGUE LIFE (NORMALIZED) | | |
|---------------------|-------------------|-------|-----------------------------------|---------------------------|-----------|-------|
| | Package | Board | | TEST | SRS MODEL | ERROR |
| 0.76 mm (30 mil) | 0.64 | 0.64 | 20.1 | 1 | 1 | 0.0% |
| | 0.76 | 0.76 | 16.6 | 1.44 | 1.71 | 18.8% |
| | 0.64 | 0.76 | 18.3 | 0.84 | 0.87 | 3.6% |
| | 0.76 | 0.64 | 18.3 | 1.77 | 1.75 | -1.1% |
| 0.97 mm (38 mil) | 0.64 | 0.64 | 30.8 | 1.28 | 1.22 | -4.7% |
| | 0.64 | 0.76 | 28.2 | 1 | 1.17 | 17.0% |
| | 0.76 | 0.76 | 26.6 | 1.69 | 1.92 | 13.6% |

Table 1: Effect of board and package pad sizes on PBGA solder joint life.

Table 1 gives solder joint fatigue lives for several combinations of ball, package and board pad sizes for 1.5-mm pitch, 225 I/O PBGAs on FR-4. The test data is after Ejim et al. (1995/96). Package pads were solder-mask-defined and board pads were non-solder-mask-defined. Accelerated thermal cycling conditions were 0°C to 100°C, with 5-minute dwells and at a test frequency of 72 cycles/day. The test results are normalized as in the original publications by Ejim et al. (1995/96). Since joint heights were not available, we used a truncated sphere approximation to estimate height based on solder volume and pad sizes. This spherical approximation technique has been found to work well for light packages. The SRS life predictions capture reliability trends and pad size effects accurately, with predictions being off the test results by at most 19%. Conclusions from the test data and life predictions in Table 1 are:

- Comparing the first four and last three rows in Table 1, 38 mil balls provide for an increase in fatigue life from 0% to 70-90% (compared to 30 mil balls).
- Comparing rows 1 and 2, or rows 5 and 7, increasing the pad sizes from 0.64 to 0.76 mm (i.e. +19%) on both the board and package sides increases life by 30 to perhaps as much as 70%. The solder joint height has decreased but the associated loss of life is compensated by an increase in the solder joint load bearing and crack area on the package side.
- Comparing rows 1 and 3, an increase in pad size on the board alone results in a shorter fatigue life because of the decrease in standoff height.
- Comparing rows 2 and 4, a slightly smaller pad on the board side improves attachment reliability. A similar conclusion was reached by Elenius et al. (1999) for flip-chip type solder joints with an optimum diameter of 0.35 mm on the board side when the pad diameter on the chip side is 0.45 mm.

5. Cavity-Down BGA Data

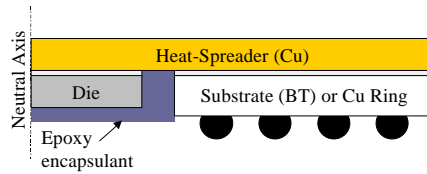


Figure 3: Schematic cross-section of cavity-down BGA.

| Component | α_{comp} (cycles) | | Ratio Test / SRS Pred. | $N_{50\%}$ (cycles) IPC-SM785 |
|---|---------------------------------|----------------|---------------------------|----------------------------------|
| | Test | SRS Prediction | | |
| 560 I/O SBGA | 2676 | 2946 | 1.101 | 2398 |
| 352 I/O SBGA | 3522 | 4007 | 1.138 | 4198 |
| 540 I/O EBGA: 1 mm BT, Single Reflow | 8157 | 9953 | 1.220 | 62088 |
| 540 I/O EBGA: 1 mm BT, Double Reflow | 8695 | 11880 | 1.366 | 165162 |
| 540 I/O EBGA: 0.75 mm BT, Single Reflow | 8328 | 10640 | 1.278 | 62088 |
| 540 I/O EBGA: 0.75 mm BT, Double Reflow | 9271 | 11820 | 1.275 | 165162 |

Table 2: Comparison of measured and predicted fatigue lives for cavity-down BGAs.

Table 2 gives a comparison of measured and predicted characteristic lives for six different cavity-down BGA assemblies (see schematic in Figure 3): 352 and 560 I/O SuperBGAs (SBGAs); 540 I/O Enhanced BGAs (EBGAs) with 0.75 mm or 1 mm BT assembled by single or double-reflow onto FR-4 boards. The SBGA data is from the NASA-JPL's BGA consortium (Ghaffarian, 1997-99), the EBGA data is from Ejim et al. (1997). The SRS life predictions are based on the model centerline. Further details on the cavity-down BGA models will be presented elsewhere (Clech, 2000).

The 1.27 mm pitch SBGAs were 352 I/O (35 mm square) and 560 I/O (42 mm square) BGAs on 59 mil thick FR-4. Accelerated thermal conditions were from -55 to 125°C with 10 to 15°C/min. ramps, 20-minute dwells and a cycle duration of 68 minutes (21.176 cycles/day). The measured effective CTE of SBGA components was 16.3 ppm/°C, the in-plane CTE of the FR-4 board was measured at 14.4 ppm/°C. Detailed information on the JPL's test vehicles, test procedures, failure analysis and failure data can be found in publications by Ghaffarian (1997-99). Using accurate CTE values is important because the package-to-board CTE mismatch is small: $\Delta\alpha = 16.3 - 14.4 = 1.9$ ppm/°C. Even though the package is well matched to the boards, cyclic shear strains $\Delta\gamma$ in the corner joints are large because of the large Distance to Neutral Point (DNP) for the corner joints and the large temperature swings ΔT :

- For the 352 I/O SBGAs: $\Delta\gamma = \frac{\text{DNP}_{\text{max}} \Delta\alpha\Delta T}{h_S} = \frac{0.8838 \times 1.9 \cdot 10^{-6} \times 180}{19.2 \cdot 10^{-3}} = 1.57\%$
- For the 560 I/O SBGAs: $\Delta\gamma = \frac{\text{DNP}_{\text{max}} \Delta\alpha\Delta T}{h_S} = \frac{1.131 \times 1.9 \cdot 10^{-6} \times 180}{19.2 \cdot 10^{-3}} = 2.01\%$

In these calculations of maximum cyclic shear strains, h_S is the component standoff height. Past experience with leadless components such as LCCCs suggests that cyclic shear strains of the order of 1% raise a red flag since they lead to failures in a few hundred cycles, or 1000-2000 cycles when the solder crack area is sufficiently large, which is the case with SBGAs. The size of SBGA packages may be a reliability-limiting factor.

The 540 I/O Enhanced BGAs (EBGAs) assemblies were tested by Ejim et al. (1997) under thermal cycling conditions from 0°C to 100°C with dwell times of about 5 minutes and a test frequency of 72 cycles per day. For single reflow assemblies, the standoff height was 0.46 mm. For double reflow assemblies, the joints were stretched to a height of 0.68 mm. The average board-to-component CTE mismatch was $\Delta\alpha = 1.0$ ppm/°C. For further information on the EBGA tests, the reader is referred to the original publication by Ejim et al. (1997).

The comparison of test and life predictions in Table 2 leads to the following conclusions:

- In the case of SBGAs, for which we had accurate input parameters, the discrepancy between test results and the SRS predictions is 10 to 14%.
- In the case of EBGAs, some of the SRS input parameters were not known accurately and the discrepancy is slightly larger, in the range 22% to 37%. Simplifications in the package modeling technique contribute to the discrepancy as well.
- Nevertheless, the agreement between test results and SRS life predictions is thought to be acceptable since the accuracy of fatigue life models is at best within a factor of two times.

Table 2 also gives cycles to 50% failures - i.e. $N_{50\%}$, which is close to the characteristic life of Weibull distributions - as obtained from the IPC-SM785 life prediction model:

- For the SBGAs under conditions -55°C to 125°C, the agreement with the test data is very good.
- For the EBGAs under conditions 0°C to 100°C, the IPC model over-predicts fatigue lives. The discrepancy with the test data is a factor 8 to 19 times.
- The two findings above are perplexing since IPC-SM785 states that the IPC model does not apply to temperature ranges that have a cold temperature below -20°C. On the other hand, the model is supposed to apply in the range 0°C to 100°C, however, this does not seem to apply to the EBGA test and EBGA assemblies.

6. Flip-Chip Data and Underfill Effect

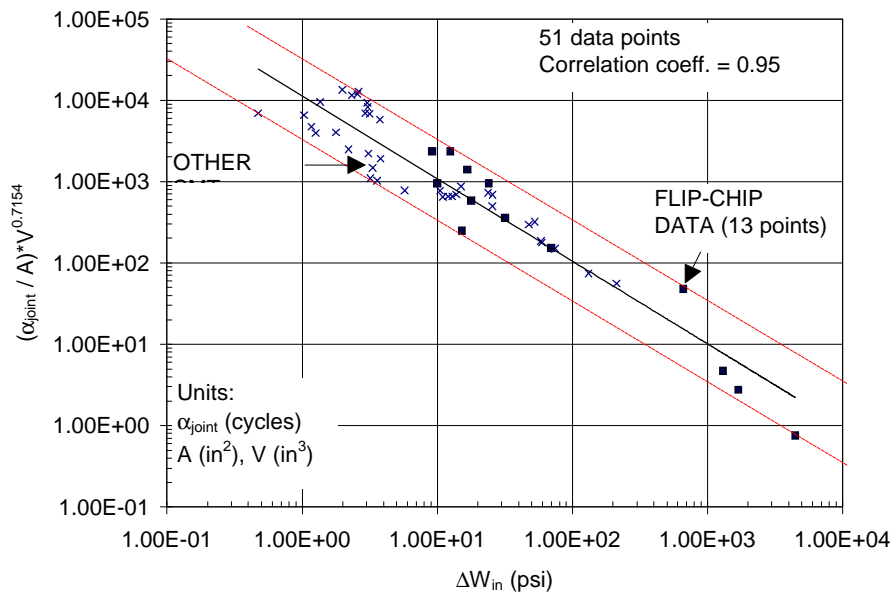


Figure 4:

| UNDERFILL | | $N_{50\%}$ (outer row) | | SOLDER STRAINS | |
|-----------|--------------|------------------------|-----------|-------------------------------|--------------------------|
| MATERIAL | CTE (PPM/°C) | TEST | SRS MODEL | SHEAR ($\Delta\gamma_{in}$) | TENSION (ϵ_z) |
| NONE | NA | 50 | 58 | 13.32% | 0 |
| B | 28 | 2800 | 2514 | 0.81% | 0.08% |
| A | 58 | 850 | 2232 | 0.92% | 0.68% |

Table 3: Test data and life predictions for flip-chip joints with and without underfill.

In the past, we have shown that the correlation of flip-chip or very fine-pitch solder joint failure data requires the use of a volume correction factor to account for the fact that small size solder joints have a higher fatigue

resistance than large joints (Clech, 1998). The results of that study are shown in Figure 4, which is similar to the original SRS correlation plot (Figure 1), but with an added volume (V) correction factor on the vertical axis. The exponent of the volume correction factor was obtained empirically to bring together failure data for conventional SMT assemblies and flip-chip assemblies with and without underfill. This approach was validated successfully for fine-pitch ceramic CSP assemblies. In this section, we pursue the validation of the correlation in Figure 4 by applying the SRS model, with volume correction factor, to other flip-chip assemblies with and without underfill. The new flip-chip data is from Nysaether et al. (1998). Corner joints of silicon die on FR-4 had a maximum DNP of 4.1 mm. Thermal cycling was between -55°C and 145°C at a test frequency of 48 cycles/day and with 30-minute dwells. Test vehicles had bare die or underfilled die with underfill materials A and B. The CTEs of the underfill materials below their glass transition temperatures are given in Table 3. Predicted and measured median cycles to failure ($N_{50\%}$) are also given in Table 3 as well as calculated inelastic shear strains and axial strains in the solder joints.

- In the case of bare die and flip-chip with underfill B, the agreement between the test results and the SRS model is excellent. The CTE of underfill B is close to the CTE of solder (24 ppm/°C), thus, axial strains in the joints are negligible and have very little impact on the fatigue life. Here, the agreement between the test data and the SRS model with volume correction factor is excellent.
- In the case of flip-chip with underfill A, the SRS model, which does not include the effect of axial strains in the solder joints, overestimates fatigue life by a factor of 2.6X. The discrepancy is due in part to large strains in the z-direction (because of the large CTE mismatch between underfill A and solder) that further reduce the fatigue life. Underfill delamination, which is a competing failure mode for underfilled flip-chip assemblies, may also contribute to the discrepancy between measured and predicted solder joint lives.

7. BLP CSP Data - Effect of Board and Package CTE

| YEAR | PACKAGE | LEADFRAME | CTE (PPM/°C) | REFERENCE |
|------|--------------|-----------|--------------|-------------------|
| 1996 | 20 I/O S-BLP | Alloy 42 | 3.6-4.5 | Kim et al., 1996 |
| 1997 | 28 I/O C-BLP | Alloy 42 | 6.3 | Choi et al., 1997 |
| 1998 | 28 I/O BLP | Alloy 42 | 8.6 | Choi et al., 1998 |
| 2000 | 54 I/O BLP | Copper | 11.8 | Choi et al., 2000 |

Table 4: Effective CTE of BLP packages (data by Kim / Choi et al., 1996-2000).

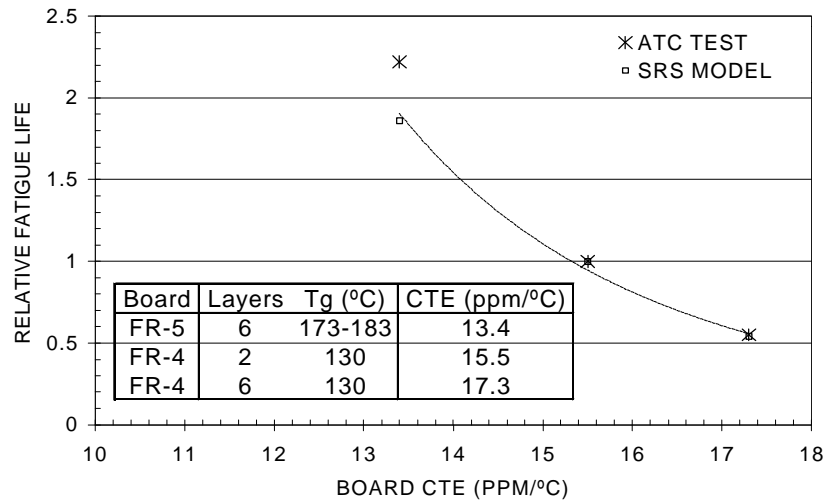


Figure 5: Effect of board CTE on BLP joint life (data / modeling by Choi et al., 1998).

The Bottom Leaded Plastic (BLP) package is a leadframe CSP that can be described as a die-up, shrunk TSOP without external leads. The BLP is similar to the JEDEC standard Small Outline No-lead (SON) CSP. A summary of BLP solder joint reliability results is presented here. The data constitutes a textbook example of a package supplier intent on optimizing package properties, as well as providing board selection guidelines, to increase solder joint reliability.

Table 4 gives measurements of effective CTEs of BLP packages since 1996. In the 1996-98 time-frame, the leadframe design and molding compound were optimized to increase the package CTE from 3.6 ppm/°C to 6.3 ppm/°C and then 8.6 ppm/°C. The year 2000 results give an effective CTE of 11.8 ppm/°C that was achieved by switching from an Alloy 42 to a copper leadframe. This last improvement provides for a 2X increase in solder joint life (Choi et al., 2000).

Figure 5 shows normalized solder joint life for a 28 I/O BLP with a CTE of 8.6 ppm/°C as a function of board CTE under accelerated thermal conditions between 0°C and 100°C. The SRS predictions performed by Choi et al. (1998) are in excellent agreement with the test results. The data shows that by switching from a board with a CTE of 17.3 ppm/°C to a board with a CTE of 13.4 ppm/°C, the BLP solder joint life increases by a factor of four times. Supplier-provided data and design curves such as those shown above are of great use for physical designers to establish the solder joint reliability of their own product boards.

Conclusions

This paper gave an update of test data that was used to validate the SRS life prediction model for several types of BGA, flip-chip and CSP assemblies. The model has now been validated by over 70 experiments. The good agreement between test data and predicted solder joint lives points to the significant impact of package and board parameters (geometry and material properties) on attachment reliability. Such predictive techniques are of use for up-front design-for-reliability and to derive test acceleration factors. The accuracy of estimating acceleration factors has become critical for some BGA and CSP assemblies with lower reliability margins than conventional SMT assemblies.

Acknowledgments

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