SOLDER RELIABILITY SOLUTIONS: A PC-BASED DESIGN-FOR-RELIABILITY TOOL

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ABSTRACT

This paper presents a solder joint engineering reliability model - Solder Reliability Solutions[1] (SRS) - and its application to surface mount area-array and chip-scale assemblies. The model is validated by failure data from thirty three accelerated thermal cycling tests, and test vehicles covering several generations of component, assembly and circuit board technologies and a variety of test conditions. The SRS model has been implemented as a PC-based design-for-reliability tool that enables rapid assessment of assembly reliability in the early stages of product development.

Keywords: Solder joint fatigue, predictive modeling, design-for-reliability, area-array / chip-scale assemblies.

INTRODUCTION - WHY BE CONCERNED?

Cyclic thermal stress conditions in surface mount assemblies leads to solder fatigue. The problem is not new but concerns are growing as advances in electronics packaging place more demand on solder interconnect reliability [1-4]. With the advent of thin low-profile leaded packages, leadless area array or miniaturized electronic packages, some of the reliability issues associated with Leadless Ceramic Chip Carriers (LCCCs) on organic substrates have resurfaced. Design characteristics that may impact the fitness-for-use of modern soldered assemblies are described as follows:

- Many packages are leadless while others have short leads with limited compliance.
- Their effective Coefficient of Thermal Expansion (CTE) may be low because of the high silicon contents of shrinking packages.
- Area-array packages are increasing in size.
- The assembled packages may have a low stand-off height for miniaturization purposes.
- Chip Scale Package (CSP) assemblies are very fine pitch with micro-solder joints having smaller load bearing or crack propagation areas than conventional surface mount assemblies.

The reliability of modern soldered assemblies needs to be looked at carefully, more so than with conventional surface mount assemblies. Upfront reliability assessment using modeling and/or accelerated testing provides means to design and manufacture robust assemblies that will meet product life requirements.

Modeling is a cost-effective way to estimate solder joint reliability, although the implementation cost and resources required to run various models can vary by orders of magnitude. Engineering reliability models using finite element analysis [2, 5] or classical mechanics [3, 6-9] have been developed that enable designers to build-in attachment reliability. While the above models, and others, can be differentiated by the scope of their analytical capabilities, needed user skills and computational requirements, the approaches followed seem to converge. Common features of the above referenced models are:

- Fatigue life predictions are based on a strain energy criterion.
- The models are validated by large databases of accelerated test data for real electronic assemblies.

This paper presents the SRS model for eutectic or near-eutectic assemblies. The model was developed for peripheral leadless and leaded soldered assemblies and has since been extended to area-array [6] and CSP assemblies [8]. SRS has been implemented as a PC-based application that allows design and manufacturing engineers to focus on design-for-reliability issues and problem-solving activities.

SRS MODEL

The model builds up on the previously published Comprehensive Surface Mount Reliability (CSMR) methodology [7, 9]. CSMR was re-engineered by Mei [3] who further validated the basic approach with Thin Small Outline Package (TSOP) test data. Innovative features in SRS are:

- Bending and stretching of parts (board and component) is accounted for in the case of leadless assemblies. These effects are important for leadless area-array plastic packages and CSPs where the component flexural compliance, which depends on the package contents and construction, can provide for stress and strain relief in the solder joints.
- Inelastic strain energy is from complete hysteresis loops with different dwell times on the hot and cold sides of thermal cycles.

[1] Solder Reliability Solutions™ is a registered trademark of EPSI Inc.

- The local mismatch stress/strain response is determined from the combined and simultaneous action of solder/board and solder/lead (or component) CTE and modulus mismatches. The analysis uses a tri-layer model which also accounts for the local effects of board to lead (or component) CTE and modulus mismatches.
- Fatigue life from component test vehicles is correlated on a joint per joint basis.

Life Data Correlation

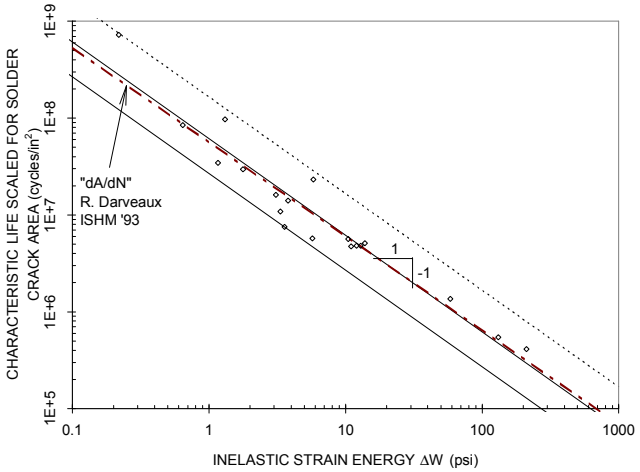

Figure 1: SRS correlation of accelerated test data.

Figure 1 shows the SRS correlation of fatigue life data from nineteen accelerated tests. The correlation gives joint characteristic lives scaled for the solder crack area versus cyclic inelastic strain energy:

$$\frac{\alpha_{JOINT}}{A} = \frac{6.149 \times 10^{7} \times C}{\Delta W^{0.998}} \qquad (1)$$

where:

- α_{JOINT} (cycles) is the characteristic life or cycles to 63.2% failures in the joint population.
- A (in^2) is the solder crack area for fully cracked, electrically open solder joints (also the minimum solder joint load bearing area).
- ΔW ($lb.in/in^3$ or psi) is the cyclic inelastic strain energy per unit volume obtained as the sum of strain energies due to global and local CTE mismatches (see section on hysteresis loops).
- C is a model calibration factor. C equals 1 for the centerline of the correlation band, 0.434 for the lower bound, and 2.7 for the upper bound.

The parameter α_{JOINT}/A (with units of cycles/in^2) is the inverse of an area crack propagation rate (in^2/cycle) and is interpreted as the number of cycles it takes for a crack, or several micro-cracks, to propagate through a unit of solder attach area.

The least squares goodness-of-fit correlation coefficient for the data in Figure 1 is 0.965. Scatter is 2.3 times below the centerline and 2.7 times above, which is typical of fatigue and of similar amplitude as in other models. The model was frozen as shown in Figure 1 and the correlation was later validated with data from another fourteen experiments (see MODEL VERIFICATION section). That is, the model is supported by thirty three experiments. The slope of the life data correlation is about -1, close to those of CSMR [7, 9] and R. Darveaux's crack growth model [2, 10]. Also shown in Figure 1 is a straight line of inverted mean propagation rates ("dA/dN") from R. Darveaux 's crack propagation model [10]. Since the difference between mean and characteristic lives is small, the fit of Darveaux 's crack growth rate to the average crack propagation rates of SRS is good. The two models are consistent and validate one another.

The test vehicles and test conditions for the nineteen experiments [11-15] that were used to develop the SRS correlation include the following:

- Components: LCCCs, Plastic Quad Flat Packs (PQFPs), TSOPs, Ceramic Leaded Chip Carriers (CLCCs), Small Outline Transistors (SOTs).
- Boards: double-sided, multilayer, FR-4 or copper-clad-invar, with in-plane CTEs over the range 8 to 21 ppm/ºC.
- Eutectic or near-eutectic (60 Sn-40 Pb) tin-lead solder.
- Test conditions: mild (25 / 65ºC) to highly accelerated (-55 / 125ºC), with dwell times from a few to 50 minutes. Test frequency was from 10 to 60 cycles/day with often different dwell times on the cold and hot sides of a thermal cycle.

Hysteresis Loops

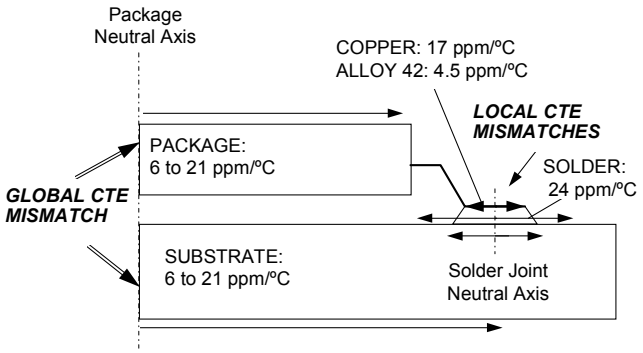

Figure 2: Global and local CTE mismatches.

The inelastic strain energy in equation (1) is obtained as the area of solder joint hysteresis loops during thermal cycling. The SRS model uses simplified one-dimensional structural models to estimate the solder joint stress/strain cycles due to global and local CTE mismatches (Figure 2).

Global mismatch refers to shear deformations of solder joints driven by thermal expansion differentials between

component and board. Because shear strains are defined as distortion angles, the shear deformation mode of leadless solder joints accounts for both in-plane shear and bending of the assembly. Local mismatch refers to deformations in the solder joint due to lateral expansion differentials between solder (24 ppm/ºC for near-eutectic tin-lead), board and leadframe (17 ppm/ºC for copper leads, 5 ppm/ºC for Alloy 42 leads) or component material.

For global mismatch, the thermal expansion differential between board and component is:

$$\Delta_G = L_D \Delta\alpha_G \Delta T \qquad (2)$$

and the largest possible shear strain at a corner joint is:

$$\gamma_{MAX} = \frac{L_D}{h_S} \Delta\alpha_G \Delta T \qquad (3)$$

where L_D is half the diagonal dimension of the component; h_S is an effective solder joint height (stand-off height for column-like joints, or half-the solder paste thickness for joints of leaded assemblies); $\Delta\alpha_G$ is the absolute value of the component to board CTE mismatch; $\Delta T = T - T_{COLD}$ is the temperature swing between the low temperature T_{COLD} on the cold side of the cycle and the current temperature T ($T = T_{HOT}$ on the hot side of the cycle). During thermal cycling, stress reduction is limited by the dwell period at T. The thermal expansion differential Δ is taken up by solder joint shear deformations (strain γ) and elastic deformations of compliant members of the assembly, that is:

$$\gamma + \frac{\tau}{\kappa} = \gamma_{MAX} \qquad (3)$$

where τ is the average solder joint shear stress and κ is the slope of stress reduction lines [16, 17] during soaks at a fixed temperature T (see Figure 3a).

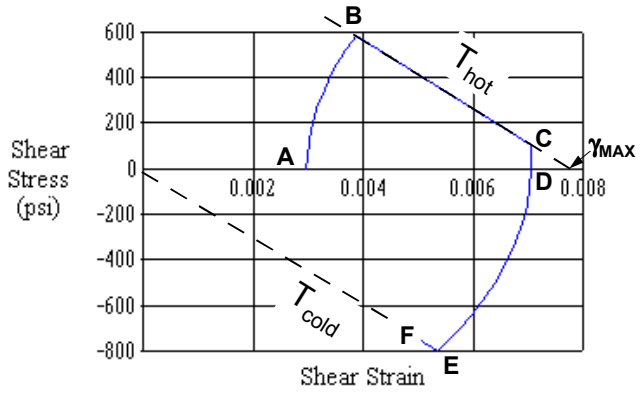

Figure 3a: Stress reduction lines,hysteresis loop calculation.

The slope κ is given as:

$$\kappa = \frac{K h_S}{A} \qquad (4)$$

where:

- K is the assembly stiffness on a per joint basis. For leadless components, K accounts for elastic deformations (board/component stretching and bending) of a slice of the assembly of width the assembly pitch. For leaded components, K is taken as the diagonal lead stiffness of a corner lead, using lead stiffness models developed by R. Kotlowitz [18, 19].
- A is the minimum solder joint load bearing area in shear, that is the minimum solder joint cross-section parallel to the board. In most cases, A is also the solder joint crack area, or fracture surface area, for an electrically open, fully cracked solder joint.

The procedure that was developed to generate approximate hysteresis loops (Figure 3a and 3b) is as follows.

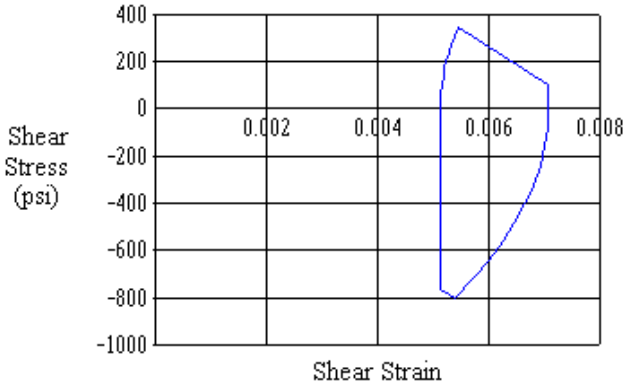

Figure 3b: Closed hysteresis loop.

Step 1: starting at an arbitrary strain level γ_A (in the range 0 to γ_{MAX}) and zero stress (point A in Figure 3a) the solder joint response during temperature ramp up is approximated by time-independent plastic deformation. Stress builds up along the path AB. Using the plastic flow rule due to Knecht and Fox [20], the stress/strain relation along AB is:

$$\gamma - \gamma_A = \left(\frac{\tau}{\tau_P}\right)^2 \qquad (5)$$

where the temperature-dependent plasticity parameter τ_P is evaluated at T_{HOT}. From linear curve-fitting of the τ_P data in [20], the plasticity parameter is given as:

$$\tau_P(psi) = \tau_P(T) = 49{,}367 - 299 \times T(^{\circ}C) \qquad (6)$$

Since point B is at the intersection of the plastic flow curve (AB) and the stress reduction line (BC) on the hot side of the cycle, the stress/strain solution at B is obtained from the following two equations:

$$\gamma_B + \frac{\tau_B}{\kappa} = \gamma_{MAX} \qquad (7a)$$

$$\gamma_B - \gamma_A = \left(\frac{\tau_B}{\tau_P(T_{HOT})}\right)^2 \qquad (7b)$$

Step 2: during the dwell period at T_{HOT}, the solder joint stress-relaxes from B to C. The stress reduction (τ_B to τ_C)

and creep strain (γ_C - γ_B) at T_{HOT} are obtained by integration of the creep rate equation[2]:

$$\dot{\gamma}_{CREEP} = A(T)\tau^n \quad (8)$$

where the stress exponent n and the temperature-dependent factor A(T) are given in the next section. After differentiating (3) with respect to time and substituting the resulting strain rate into (8), the shear stress is found to follow the following differential equation:

$$\dot{\tau} = -\kappa A(T)\tau^n \quad (9)$$

For n not equal to 1, integration of (9) gives the following equation for the stress τ_C at the end of the dwell period of duration $t_{D(HOT)}$:

$$\tau_C^{-n+1} - \tau_B^{-n+1} = (n-1)\kappa A(T_{HOT})t_{D(HOT)} \quad (10)$$

The end strain is then obtained by solving the stress reduction line equation at point C for γ_C:

$$\gamma_C + \frac{\tau_C}{\kappa} = \gamma_{MAX} \quad (11)$$

Step 3: when the thermal cycle is reversed (ramp-down), unloading from C to D is on a straight vertical line, that is:

$$\gamma_D = \gamma_C\ ,\ \tau_D = 0 \quad (12)$$

Since solder joint elastic strains are, in general, much smaller than plastic and creep strains, elastic unloading is neglected here.

Step 4: upon further temperature ramp-down, stress builds up in the opposite direction along the path of plastic flow DE. Following a procedure similar to Step 1, the stress/strain components at E are obtained at the intersection of the path DE and the stress reduction line at T_{COLD}. That is, τ_E and γ_E are solutions of the following two equations:

$$\gamma_E + \frac{\tau_E}{\kappa} = 0 \quad (13a)$$

$$\gamma_D - \gamma_E = \left(\frac{\tau_E}{\tau_P(T_{HOT})}\right)^2 \quad (13b)$$

Step 5: during the cold dwell period of duration $t_{D(COLD)}$ on the cold side of the cycle, stress is reduced from τ_E to τ_F along the stress reduction line at T_{COLD}. Similar to creep calculations in Step 2, the end stress τ_F is obtained from the following equation:

$$|\tau_F|^{-n+1} - |\tau_E|^{-n+1} = (n-1)\kappa A(T_{COLD})t_{D(COLD)} \quad (14)$$

The end strain γ_F is given by the stress reduction line equation at point F:

$$\gamma_F = -\frac{\tau_F}{\kappa} \quad (15)$$

Step 6: when temperature ramps up for the next cycle, unloading is on a straight vertical line as in Step 3. If γ_F is close to γ_A, then the loop has stabilized and is almost closed. If the loop has not closed, Steps 1 to 5 are repeated with a new starting value of the initial strain (for example, half-way between γ_A and γ_F). Loop iterations are stopped when the stress/strain cycle closes (Figure 3b) to within a specified accuracy. The loop closure accuracy, %e, is defined as:

$$\%e = \frac{|\gamma_A - \gamma_F|}{\gamma_D - \gamma_A} \quad (16)$$

where $|\gamma_A - \gamma_F|$ is the strain differential between the start and end points of a loop iteration. The strain range, γ_D - γ_A, gives the cyclic inelastic strain range (loop width) when the loop closes.

Solder Constitutive Model and Creep Rate

Since solder properties are a function of microstructure and can be affected by many parameters (e.g. cooling rate, aging, intermetallics), there is no unique constitutive model for solder joints. The constitutive model used in SRS is derived from data and analysis by Knecht et al. [20], Shine et al. [21], and Wong et al. [22]. The time-independent plasticity model is from [20, 21] and the creep rate model is derived from data in [22].

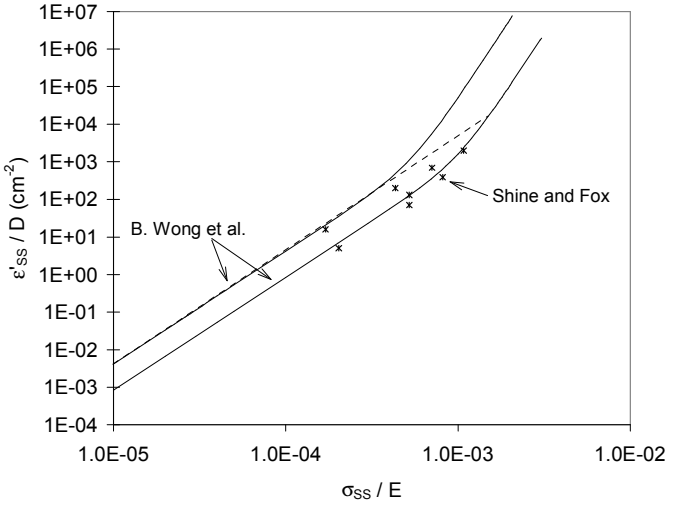

Figure 4: Steady state creep model [20] and data [18] (SS = steady state; D = Arrhenius factor in [20]).

The lower and upper bounds of steady state solder creep data compiled by Wong [22] are plotted in Figure 4. As previously shown [17], the creep data measured by Shine et al. [20] on actual solder joints fits within these bounds. Wong's creep rate equation is the sum of two creep rates, one with a stress exponent of 3, the other with an exponent of 7, as evidenced by the change of slope in Figure 3. SRS uses the upper bound of Wong's creep rates and truncates his creep equation to the first term (stress exponent of 3) to enable a fit to the creep rate equation (8). As shown by the dashed line in Figure 4, using the upper bound of Wong's data maximizes creep rates in the low stress region and provides an average fit in the knee region of the creep rate plot. In the knee region, the dashed line is above Shine et al.'s data [20]. These approximations are thought to be

[2]A circle above time-dependent variables denotes time derivatives.

acceptable since, beyond the knee region, stresses are so high that solder joint fatigue life is likely to be very short.

The creep rate equation in SRS is determined from the equation of the dashed line in Figure 4, with normal stress and strain (σ, ε) in Wong's equations converted to shear (τ, γ) through the transformations: $\varepsilon = \gamma/\sqrt{3}$, $\sigma = \tau\sqrt{3}$ [23, 24]. Thus, the stress exponent and temperature-dependent factor in the creep rate equation (8) are:

$$n = 3 \tag{17a}$$

$$A(T)(\sec^{-1}/\mathrm{psi}^3) = 7.298\times10^{13}\,\frac{1}{E^3(T)}\,e^{-\frac{5412}{T(^\circ K)}} \tag{17b}$$

where E(T) is Young's modulus of near-eutectic tin-lead [22]:

$$E(T)(\mathrm{psi}) = 1.45\times10^5(32.0 - 0.088T(^\circ C)) \tag{17c}$$

Note: temperature ramp-rates are not included in the stress/strain analysis of the present version of SRS. This is not a concern, in general, except for slow moving field conditions with very slow ramps or very short dwells. Ramp-rates in the tests that were used to establish the life data correlation were typical of single or double chamber air-to-air thermal cycling -- in the range 5 to 80°C/min -- and this did not seem to have an effect on the SRS correlation of life data. By not including creep during the temperature ramps, the analysis underestimates the initial inelastic strains but this leads to higher stresses building up, which in turn leads to larger creep rates and creep strains during the dwell periods. This is thought to be conservative for making reliability predictions because the resulting stress/strain hysteresis loop has, in general, a larger area than when creep is included during the ramps. Ramp-rates will be included in future refinements of SRS.

Stiffness Parameters

For single-sided leadless assemblies, the assembly stiffness K is the equivalent stiffness of three springs in parallel:

$$\frac{1}{K} = \frac{1}{K_1} + \frac{1}{K_2} + \frac{1}{K_3} \tag{18}$$

where the spring constants are:

- K_1 for mechanical stretching of the component.
- K_2 for mechanical stretching of the substrate.
- K_3 for bending of the assembly.

For double-sided assemblies with identical components mounted back-to-back, the substrate does not bend and the assembly stiffness is given by:

$$\frac{1}{K} = \frac{1}{K_1} + \frac{2}{K_2} \tag{19}$$

Equations (18) and (19) are derived from existing assembly stiffness formulations and mechanical analysis of LCCCs and discrete assemblies [25, 26].

For LCCC assemblies, the spring constants are:

$$K_1 = \frac{E_c^t h_c P}{L_D(1-\nu_c)} \tag{20a}$$

$$K_2 = \frac{2E_b^t h_b P}{L_D(1-\nu_b)} \tag{20b}$$

$$K_3 = (D_c + D_b)\frac{P}{L_D H^2} \tag{20c}$$

where $H = \frac{h_c}{2} + h_S + \frac{h_b}{2}$, and D_c and D_b are the component and board flexural rigidities:

$$D_c = \frac{E_c^f h_c^3}{12(1-\nu_c)},\ D_b = \frac{E_b^f h_b^3}{6(1-\nu_b^2)}. \tag{21}$$

Subscripts i = "c" and "b" are for component and board parameters, respectively. P is the assembly pitch, h_c is the component or LCCC floor thickness, h_b is the board thickness, ν_i's are Poisson's ratios, E_i^t's are Young's moduli in tension (superscript "t") and E_i^f's are Young's moduli in flexure (superscript "f")[3]. Board and component flexural rigidities are given as in Hall's axisymmetric model of LCCC assemblies [25] with the formulation for D_b assuming a substrate of infinite size. Interestingly, as the pitch is reduced, K decreases. The assembly becomes more compliant because each joint then acts on a narrower slice of the assembly.

For discrete assemblies, the spring constants are derived from the chip resistor model by Jih et al.[26]:

$$K_1 = \frac{E_c^t h_c w}{L_D} \tag{22a}$$

$$K_2 = \frac{E_b^t h_b w}{L_D} \tag{22b}$$

$$K_3 = (I_c + I_b)\frac{w}{L_D H^2} \tag{22c}$$

where w is the width of the discrete and I_c, I_b are given as:

$$I_c = \frac{E_c^f h_c^3}{12},\ I_b = \frac{E_b^f h_b^3}{12}. \tag{23}$$

Stiffness parameters for other component types, e.g.: full array PBGA and flip-chip with underfill, are discussed in the MODEL VERIFICATION section of this paper.

Example

An example of assembly stiffness calculation is given for a fine-pitch 84 I/O LCCC on a single-sided FR-4 board. The design parameters are from [16, 25]:

- Assembly: h_S = 11 mil, P = 25 mil.

[3] Accounting for differences in Young's moduli in tension and flexure is important for composite structures such as multi-layer organic boards.

- LCCC: $E_c^t = E_c^f = 37 \times 10^6$ psi, ν_c = 0.3, L_D = 0.367 in, h_c = 20 mil.
- Board: $E_b^t = E_b^f = 1.58 \times 10^6$ psi, ν_b = 0.28, h_b = 58 mil.

The calculated spring constants and assembly stiffness are:

	K_1	K_2	K_3	K
(lb/in)	72012	13547	2479	2036

The equivalent stiffness, K, is dominated by the bending term K_3 . The calculated stiffness (K = 2036 lb/in) is close to experimental values given in the range 1.7 to 2.0 lb/mil from strain-gauge measured hysteresis loops [16].

Local Mismatch Formulation

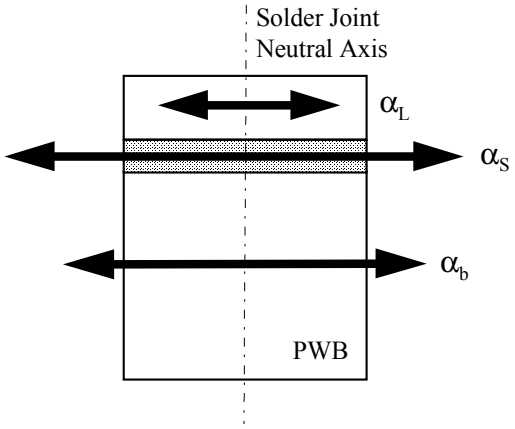

Figure 5: Local CTE mismatch tri-layer model.

Eutectic or near-eutectic tin-lead solder has higher thermal expansivity (CTE: α_S = 24 ppm/ºC) than most electronic packaging materials. Local CTE mismatch between solder and the interconnected parts of an assembly has been found to be a reliability problem [1, 3, 27]. The present formulation of local CTE mismatch is that of a simple tri-layer model (Figure 5) where the expansivity of a soft compliant layer of solder is restrained by the lower expansivity of the substrate (CTE: α_b) and that of the attached component or lead (local CTE: α_L). The local CTE mismatch problem is assumed to be independent of the global mismatch problem. In the simplified analysis below, lateral expansion of the solder joint is the driving force and only equivalent lateral strains are considered. The effect of distributed shear strains, not included here, will be considered in future improvements of the SRS model.

Normal/lateral forces F_L, F_S and F_b per unit width of the three layer model satisfy the equilibrium equation[4]:

$$F_L + F_S + F_b = 0 \qquad (24)$$

Strain compatibility gives:

$$\alpha_L \Delta T + \frac{F_L}{E_L h_L} = \alpha_S \Delta T + \varepsilon_{S,MECH} \qquad (25a)$$

$$\alpha_b \Delta T + \frac{F_b}{E_b h_b} = \alpha_S \Delta T + \varepsilon_{S,MECH} \qquad (25b)$$

where E's are Young's moduli, α's are CTEs, h's are thickness and $\varepsilon_{S,MECH}$ is the mechanical strain in solder:

$$\varepsilon_{S,MECH} = \varepsilon_{IN} + \frac{\sigma}{E(T)} \qquad (26)$$

The first term on the right hand side of (26) is the inelastic component of strain, ε_{in}, and the second term is the elastic strain. σ is the normal/lateral stress ($\sigma = F_S / h_S$) and E(T) is Young's modulus of solder as given in (17c). The solution to equations (24-26) gives:

$$\varepsilon_{IN} + \sigma\left(\frac{1}{E(T)} + \frac{1}{\kappa_L}\right) = (\alpha_{EFF} - \alpha_S)\Delta T \qquad (27)$$

where the effective local CTE, α_{EFF}, for the board and component working together against solder is:

$$\alpha_{EFF} = \frac{E_L h_L \alpha_L + E_b h_b \alpha_b}{E_L h_L + E_b h_b} \qquad (28)$$

and the local stiffness parameter κ_L is:

$$\kappa_L = E_L \frac{h_L}{h_S} + E_b \frac{h_b}{h_S} \qquad (29)$$

Equation (27) is that of stress reduction lines for the local mismatch problem, similar to equation (3) for global mismatch. The corresponding inelastic strain energy is the area of hysteresis loops calculated with the same procedure as for global mismatch hysteresis loops. Note that, from equation (27), the slope of local mismatch stress reduction lines has a slight temperature dependence.

MODEL VERIFICATION

Castellated LCCCs

The model was applied to 20, 28 and 68 I/O castellated LCCCs on 0.062" FR-4 with life cycle data and failure analysis in [28-30]. The experiments were part of a solder joint modeling round-robin conducted by Jet Propulsion Laboratory (JPL). Test conditions were those of NASA's thermal cycle test: -55ºC to 100ºC at a frequency of 6 cycles/day.

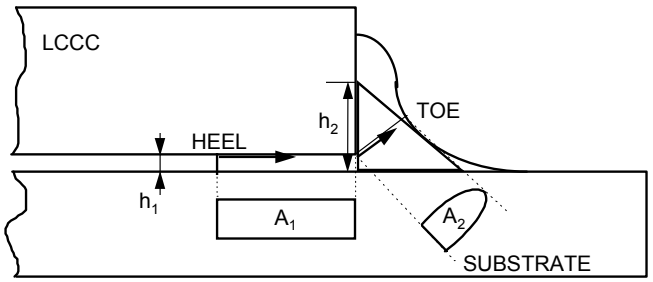

Figure 6: Castellated LCCC solder joint parameters.

[4]Subscripts used are: "L" for component or lead parameters, "S" for solder and "b" for the board or substrate.

Castellated LCCCs (Figure 6) have a low stand-off height (h_1) and toe fillets that run up the castellations. JPL's test results and failure mode analysis indicate that the solder volume and the toe fillet geometry have a significant impact on fatigue life [28, 29]. Solder joint cracking initiates in the heel fillet under the component and propagates under the LCCC termination (crack area A_1). Crack growth then proceeds at a slower rate through the outer toe fillet, at close to a 45º angle. Provided that solder volume is large enough, a significant fraction of the fatigue life is spent propagating cracks through the toe fillet (crack area A_2).

Solder joint life predictions were made by running the model twice to determine two characteristic lives:

1. α_1 for crack propagation along the thin solder layer under the LCCC termination, using the joint parameters h_1 and A_1 as input to the model.
2. α_2 for crack propagation through the toe fillet, using the fillet parameters h_2 and A_2 as input to the model.

The parameters h_1, A_1 and A_2 are estimated from solder joint cross sections and crack areas. h_2 is an effective fillet height parameter determined empirically as the height of the largest right isosceles triangle that can fit in a cross-section of the solder joint through the vertical center plane of the castellation, typically with the hypotenuse tangent to the fillet meniscus (see Figure 6). The latter rule of thumb, due to Wen et al. [28-30], was implemented in JPL's finite element model [28] and gave LCCC joint life predictions in excellent agreement with test results. The solder joint input parameters, SRS life prediction results, and predicted crack propagation rates are tabulated below:

FATIGUE LIVES (CYCLES)		**68 I/O**	**28 I/O**	**20 I/O**
TEST	α_{test}	97	690	678
PREDICTED (SRS)				
under component	α_1	41	78	119
through fillet	α_2	56	590	358
TOTAL	$\alpha = \alpha_1 + \alpha_2$	97	669	477
	ERROR	0.%	-3.%	-30.%

CRACK GROWTH RATES (10^{-6} in^2 / cycle)		**68 I/O**	**28 I/O**	**20 I/O**
under component	A_1 / α_1	29.1	11.5	8.8
through fillet	A_2 / α_2	6.0	0.8	0.9
	Ratio	4.9	14.3	10.0
Parameters				
	A_1 (x 10^{-4} in^2)	12.0	9.0	10.5
	h_1 (mil)	1.4	1.6	1.4
	A_2 (x 10^{-4} in^2)	3.3	4.7	3.2
	h_2 (mil)	21.0	33.0	23.6

The 68 I/O LCCC test results were used for model calibration (C = 1.03). Predicted life for the 28 I/O LCCCs is in very good agreement with the measured characteristic life (-3 % error). For the 20 I/O LCCCs, the life prediction is slightly conservative (-30 % error) but still in good agreement with test results. Sources of error include assembly variability, simplifications inherent to the SRS model, possible uncertainties in input parameters and reduced confidence in the measured characteristic life due to a smaller sample size: n = 8 components for the 20 I/O test versus n = 31 and 15 for the 28 I/O and 68 I/O tests, respectively. The tabulated crack growth rates are predicted average crack propagation rates. The data suggests that crack growth in the toe fillets is 5 to 15 times slower than in the thin solder layer under the LCCC terminations, in agreement with failure mode analysis results [28, 29].

Solder volume and fillet size effects may be significant for other leadless assemblies with low stand-off height, for example, passive devices (chip resistors and capacitors) where the solder layer under the bottom side terminations can be very thin. The techniques described above for reliability modeling of castellated LCCC solder joints are thought to apply to small discrete assemblies.

Alloy 42 and Copper TSOPs

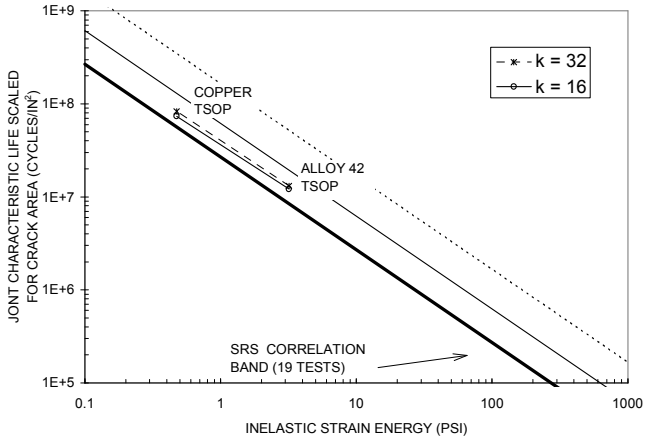

Figure 7: Fit of 32 I/O TSOP test data to the SRS model.

The SRS model was then applied to 32 I/O Type I TSOPs with Alloy 42 or copper leadframes mounted on FR-4. Model input parameters, except for the crack area but including diagonal lead stiffness, were obtained from [31]. Thermal cycling test conditions were: 0ºC to 100ºC, 5 minute dwells. Since there was little solder under the foot of leads, the solder crack area was taken as the heel crack area alone from the point where cracks initiate in the heel fillet down to the lead foot at the end of the bend (estimated as A = 1.43×10^{-4} in^2 from cross-sections of similar test vehicles in [1]).

The fit of the TSOP test data to the SRS model is shown in Figure 7. Since component failure statistics were given for TSOP side separation, the two-parameter (2P) Weibull characteristic lives (α_{COMP} = 1298 for Alloy 42, 6459 for copper [31]) were converted to joint characteristic lives, α_{JOINT}, using the transformation [9]:

$$\alpha_{JOINT} = \alpha_{COMP} \times k^{1/\beta} \quad (30)$$

where β is the shape parameter of the 2P Weibull distribution of failures (β = 9.5 for the Alloy 42 group, 5.7 for the copper group in [31]) and k is the number of component joints most susceptible to fail. We used k = 16 since the joints of a Type I TSOP fail by "zipper" effect (side separation) within a narrow range of cycles. Figure 6 shows that the fit of the data to the SRS correlation band is about the same if we use k = 32 to account for joints being damaged on both sides of the component.

The data fits well within the original SRS correlation band. From calculated strain energies, the ratio of predicted solder joint fatigue lives for copper and Alloy 42 TSOPs is 5.2, in agreement with a five times improvement reported in [31] for copper versus Alloy 42 leadframes. These results are specific to the components and test vehicles that were thermal-cycled in [31] and attachment reliability needs to be evaluated on a case-by-case basis for other TSOP assemblies.

PBGA Assemblies

Figures 8 and 9 are schematics of a full array Plastic Ball Grid Array (PBGA) assembly and the package multilayer construction (six layers) in the die area. Joints under the edge of the die fail first during thermal cycling and parameters with the greatest impact on attachment reliability are (see for example [2, 32-34]): pad diameter, laminate thickness, die size and thickness, and solder joint height. The application of SRS to full-array PBGA assemblies was presented in [6, 35]. The equations to determine effective package CTEs for global and local mismatch and assembly stiffness parameters are given below and the validity of the PBGA model is demonstrated with additional test data.

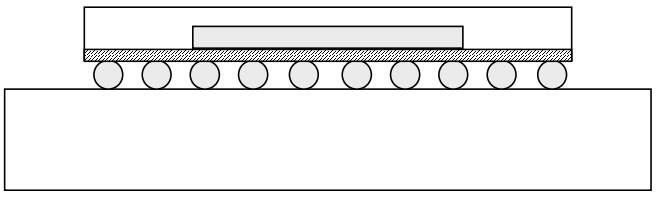

Figure 8: Schematic of full-array PBGA assembly.

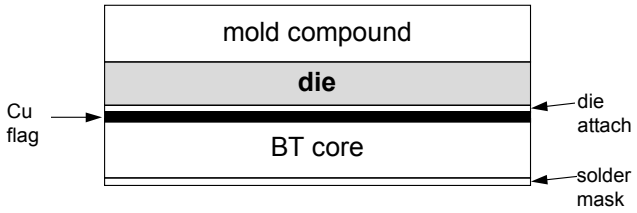

Figure 9: Schematic of multilayer construction in die area.

Since the solder joints under the edge of the die are the most susceptible to failure, we need to determine package equivalent properties (CTEs, Young's moduli) in the die area. These properties are then used in the LCCC assembly model where the LCCC package was assumed to be a homogeneous material.

Effective CTEs of PBGA Packages

For global mismatch, the effective package CTE on the bottom side of the package is obtained from thermal stress analysis of the die area multilayer construction (Figure 9) subject to a temperature swing ΔT. The effective package CTE for the global mismatch problem is:

$$\alpha_G(\text{PBGA}) = \frac{\varepsilon_X(\text{bottom})}{\Delta T} \quad (31)$$

where ε_X(bottom), the total radial strain (mechanical + thermal) on the bottom side of the PBGA - i.e., what the solder joints see - is obtained by straight application of Hall's thermal stress model for axi-symmetric multilayer stacks [36]. Hall's model was selected because it accounts for stretching and flexing of the multilayer stack, both of which are important deformation modes during global thermal expansion mismatch of PBGA assemblies [37]. The input parameters required to calculate α_G(PBGA) are thickness, Young's modulus, Poisson's ratio and CTE of each layer and material, i.e. a total of 4 parameters x 6 layers = 24 parameters.

For local mismatch alone, flexing of the package is insignificant and the effective package CTE, α_L, is approximated by a simple rule of mixtures:

$$\alpha_L = \sum_{i=1}^{6} E_i h_i \alpha_i \Big/ \sum_{i=1}^{6} E_i h_i \quad (32)$$

where h_i is the thickness, and E_i and α_i are Young's modulus and the CTE of the i^{th} layer material. Layers of the multilayer stack are numbered i = 1 to 6 starting at the bottom of the stack but, for local mismatch calculations, the first layer (solder mask) is replaced by a copper mounting pad.

Effective Mechanical Properties of PBGA Packages

In order to use the LCCC assembly stiffness formulas (equations 20a and c), we need to determine an effective Poisson's ratio (ν_c) and effective Young's moduli of the package in tension and flexure (E_c^t , E_c^f).

The effective Poisson's ratio is obtained by a simple rule of mixtures, a well accepted technique in mechanics of composite materials [38]:

$$\upsilon_c = \sum_{i=1}^{6} \upsilon_i h_i \Big/ \sum_{i=1}^{6} h_i \quad (33)$$

For the global mismatch problem, the effective Young's moduli of the package are obtained by using the additivity property of the stretching and bending rigidities of individual layers of the multi-layer stack [39]:

$$\frac{E_c^t h_c}{1-\upsilon_c} = \sum_{i=1}^{6} \frac{E_i h_i}{1-\upsilon_i} \quad (34)$$

$$\frac{E_c^f h_c^3}{12(1-\upsilon_c)} = \sum_{i=1}^{6} \frac{E_i h_i^3}{12(1-\upsilon_i)} \qquad (35)$$

For the local mismatch problem, the effective Young's modulus of the package, E_L, is obtained by a simple rule of mixtures:

$$E_L = \sum_{i=1}^{6} E_i h_i \Big/ \sum_{i=1}^{6} h_i \qquad (36)$$

where the first layer of the stack (i = 1) is the attachment copper pad.

PBGA Results

Reference [6] includes detailed applications of the PBGA model that need not be repeated here. The SRS model was validated with five PBGA accelerated tests and it was shown that SRS accurately captures the effects of pad diameter, die thickness, BT thickness and stand-off height [6]. The fit of additional test data to the SRS model is shown below (Figures 10 and 11).

The PBGA model was applied to nine 225 I/O PBGA datasets from design-of-experiments reported in [32-35]. Design variables included stand-off height, die size and thickness, BT thickness, die attach modulus and pad size. As shown in Figure 10, the nine datasets fit within the SRS correlation band. Data points shown as circles are from [32], those shown as triangles are from [33, 35]. For the conversion of component characteristic lives to joint characteristic lives (equation (30)), we used k = 24, assuming that the 24 joints in the row under the edge of the die are as likely to fail as the highly stressed "corner" joints under the die corners.

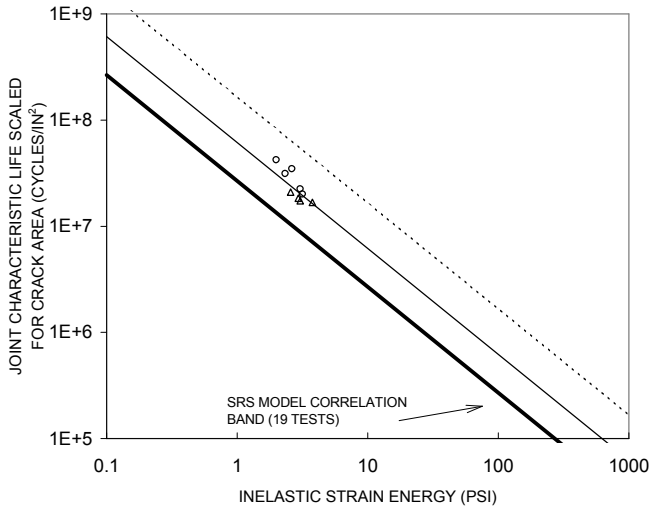

Figure 10: Fit of 225 I/O PBGA data to the SRS model.

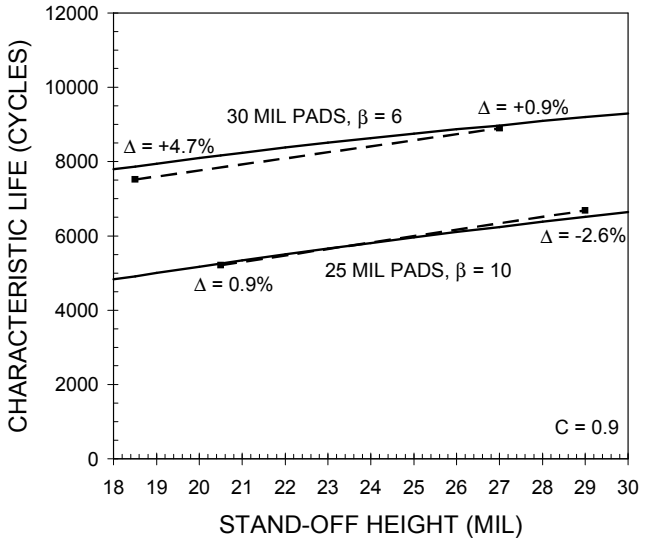

Figure 11: PBGA stand-off height effects.

Figure 11 shows the effect of stand-off height on solder joint characteristic lives (on a per component basis). Solid lines are model predictions, dashed lines are measured characteristic lives [33]. For each pad size (25 and 30 mil diameters), solder volume was kept constant and the PBGA stand-off height was increased by a double-reflow process [33]. The model fits the test data with less than 5% errors. The measured and predicted life improvements are much less than would be predicted by Coffin-Manson type relationships due to local mismatch contributions to solder joint fatigue. Similar conclusions were reached in [5, 32].

The full-array PBGA model can easily be extended to perimeter-array PBGAs. Solder joints in the row closest to the die are still expected to fail first but fatigue lives will improve because of reduced damage due to local mismatch. This effect is apparent in equation (32) where the local mismatch effective CTE, α_L, will increase away from the die, thanks to an increased contribution from the molding compound CTE.

CHIP SCALE PACKAGE APPLICATIONS

The SRS model has been extended to micro-BGAs and flip-chip with underfill assemblies [8, 40]. An overview of the mechanical models that were developed for these two technologies is given below. The micro-BGA results are in agreement with conclusions drawn from finite element studies. Predicted shear strains in the flip-chip underfill layer agree with strains derived from moiré field displacements.

Micro-BGAs

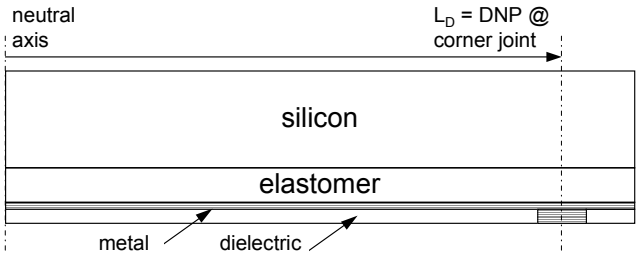

Figure 12: Schematic of micro-BGA package model.

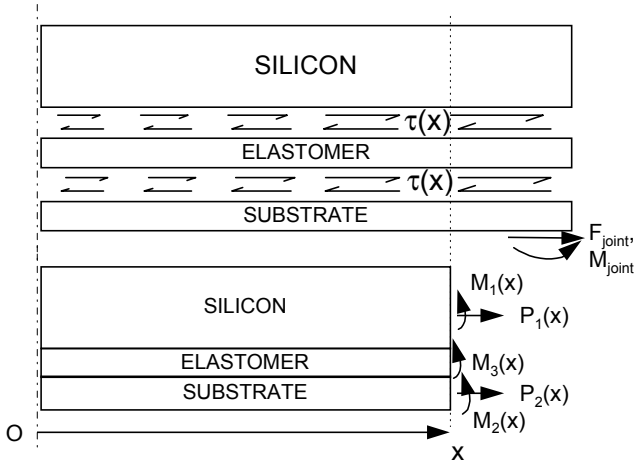

Figure 13: Internal stresses in micro-BGA package.

Figure 12 is a schematic of a micro-BGA package, where a low modulus compliant elastomer layer provides for decoupling between the silicon die and the package substrate (metal layers + dielectric). During thermal cycling, the compliant elastomer layer, with Young's modulus of a few hundred psi, is essentially in shear. Shear is driven by the CTE mismatch between the die and the package substrate, as well as external forces and moments that the solder joints exert on the package. Figure 13 shows the shear stress distribution, $\tau(x)$, in the elastomer layer, forces and moments exerted by the solder joints (F_{joint}, M_{joint}) and internal forces and moments ($P_i(x)$, $M_i(x)$) in a vertical cross-section of the package. Stresses and strains in the micro-BGA package are solved for by using existing theories of multilayer stacks and adhesive bonds. Details of the micro-BGA model are presented in [40]. The effective package CTE that is seen by the solder joints is derived from calculated strains on the bottom side of the package. For assembly stiffness calculations, the stretching and bending stiffness of the package are obtained as functions of chip size, geometry and material properties of the different layers of the package.

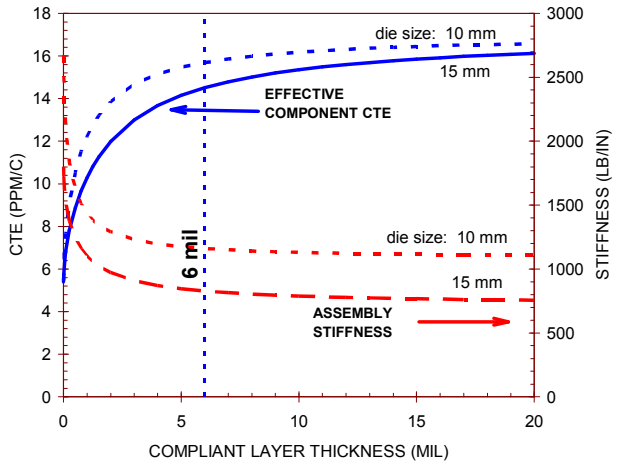

Figure 14: Micro-BGA effective CTE and assembly stiffness as a function of elastomer layer thickness.

The micro-BGA model was applied to a generic micro-BGA mounted on a 0.062" FR-4 board and with a 15 mil thick die. Material properties that were used are from [41]. Figure 14 shows the effective package CTE and assembly stiffness as a function of thickness of the compliant elastomer layer. The effective package CTE increases and the assembly stiffness decreases as the elastomer thickness increases. The elastomer layer has to be thick enough to provide an effective package CTE that is close to the CTE of FR-4 boards. For a thickness of 6 mil, the effective CTE is in the range 15.7 ppm/C (10 mm die) to 14.5 ppm/C (15 mm die). Beyond 6 mils, incremental gains in effective CTE and assembly compliance are limited. Nevertheless, with a minimum thickness of the compliant elastomer, the package-to-board CTE mismatch and the assembly stiffness are greatly reduced when compared to the situation of bare chips on FR-4.

Results of the above parametric study are in agreement with the conclusions of finite element studies in [41] and suggest that the micro-BGA model quantifies the chip-to-board decoupling well. As with PBGAs, there is a chip size effect, the impact of which, as well as other parameters, have to be evaluated on a case-by case basis. Further verification of the micro-BGA model will be conducted as assembly reliability data becomes available.

Flip-Chip with Underfill

The solder joint life improvement mechanism in flip-chip assemblies is easily conceptualized. Since the in-plane thermal expansion mismatch between die and substrate is taken up by shear of the solder joints *and* of the underfill layer, the solder joints see lesser strains than in bare chip assemblies. To a first order, mechanical coupling between the die and substrate is controlled by the shear stiffness of the underfill layer. Thus, a higher modulus underfill material provides for improved coupling and reduced shear

strains on the solder joints. The model that was developed for flip-chip with underfill [8] assumes that the CTE of the underfill material is close to that of solder (as is the case in most underfill assemblies) so the joints are not stretched in the out-of-plane direction.

Underfill Model

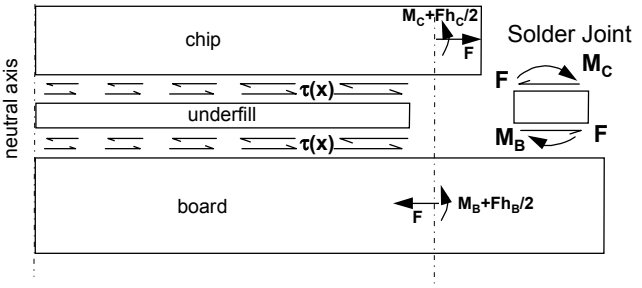

Figure 15: Interfacial shear stresses at die/underfill and substrate/underfill interfaces.

Figure 15 shows the assumed distribution of shear stresses, $\tau(x)$, at the underfill/die and underfill/substrate interfaces, as well as the shear forces and bending moments (F, M's) exerted by solder joints on the die and substrate. The solution of the strength of materials problem depicted in Figure 15 is obtained by combining Hall's model of LCCC assemblies [25] and Suhir's theory of multilayer stacks and adhesive bonds [42]. The interfacial shear stress distribution in the underfill layer is found to follow a hyperbolic sine. The solder joint shear strain and shear force are found to obey the following stress reduction line equation:

$$h_S\gamma + \frac{F}{K_U} = \frac{1}{R}L_D\Delta\alpha_G\Delta T \qquad (37)$$

where:

- K_U is the assembly stiffness of the assembly with underfill.
- R is a strain or CTE mismatch reduction factor.

K_U and R depend on the thickness and material properties of each layer of the tri-layer stack model, as well as assembly pitch and chip size. As shown in [8], when the modulus of the underfill material goes to zero, K_U converges to the assembly stiffness for an assembly without underfill (equations (18) and (20a-c)) and the strain reduction factor R goes to 1. K_U is larger than the assembly stiffness K for an assembly without underfill because mechanical coupling provided by the underfill layer stiffens the assembly. Fortunately, this decrease in compliance is offset by a large reduction in the applied strain (R >> 1, in general, with adequate selection of the underfill modulus).

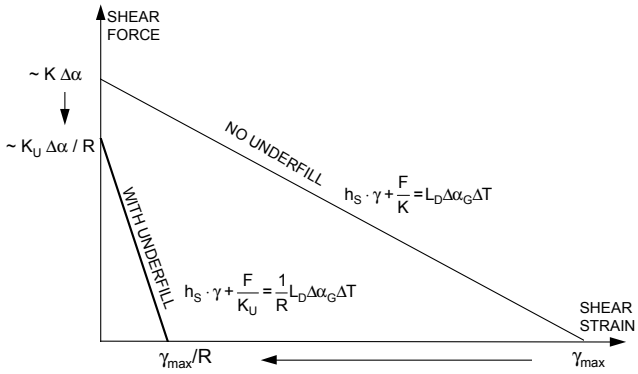

Figure 16: Solder joint isothermal stress reduction lines for assemblies with and without underfill.

The assembly stiffness, K_U, the effective global CTE mismatch $\Delta\alpha_G/R$ and the stress reduction line equation (37) are used to generate solder joint hysteresis loops. Figure 16 is a schematic of isothermal stress reduction lines in the force versus strain plane. For assemblies without underfill, the maximum applied strain is $\gamma_{max} = \frac{L_D\Delta\alpha_G\Delta T}{h_S}$, the maximum applied force is proportional to $K\Delta\alpha_G$, and the strain energy, or area of the triangle under the stress reduction line, goes as $K(\Delta\alpha_G)^2$. For the same assembly with underfill, the maximum effective strain that is seen by the solder joints is γ_{max}/R, the maximum shear force goes as $K_U\Delta\alpha_G/R$ (which is less than $K\Delta\alpha$, in general), and the strain energy goes as $K_U(\Delta\alpha_G/R)^2$. Using a strain energy criterion for solder fatigue, the mechanics of solder joints suggest a potentially significant improvement in fatigue life for assemblies with underfill compared to assemblies without underfill.

Application and Verification of the Underfill Model

The underfill model was applied to a silicon on ceramic test vehicle for which moiré displacements fields were measured by B. Han et al. [43]. Young's modulus for the underfill material (E_U) was not known so the model was run for E_U in a range typical of existing materials (E_U = 0.9, 1.4 and 2.0 Mpsi). Thermal loading was ΔT = -80ºC from 102ºC to room temperature.

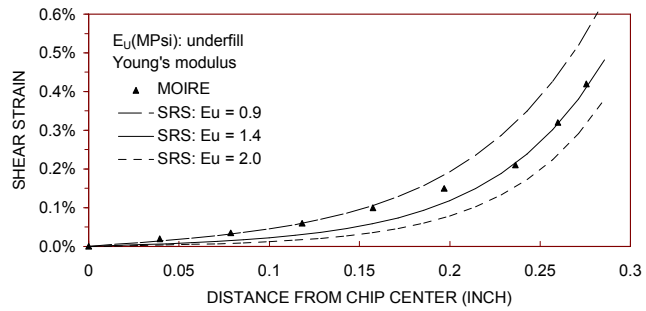

Figure 17: Shear strain distribution in underfill layer of silicon-on-ceramic test vehicle (ΔT = -80ºC).

The predicted shear strain distribution in the underfill layer, from the center to the edge of the chip, is plotted in Figure 17. Average shear strains from moiré measurements are shown as triangles. The trend of predicted strains agrees with the data. In the high strain region towards the edge of the chip, the model fits best for E_U = 1.4 Mpsi. Sources of discrepancy include simplifications inherent to the strength of materials approach, uncertainties in material properties, the possible temperature dependence of underfill properties, and the absence of end fillet effects in the model. The resolution of measured displacements (U and V fields in the horizontal (X) and vertical (Z) directions, respectively) and the approximation of the V-displacement cross-derivative as: $\frac{\partial V}{\partial X} \approx 0$ to obtain average shear strains in the thin underfill layer may also contribute to the discrepancy, especially in the low strain region. The agreement between predictions and experiment is good and gives support to use of the model for further analysis and parametric studies [8]. The strain reduction factor, R, and the resulting effective CTE mismatches, $\Delta\alpha/R$, are tabulated below for the three assumed values of E_U:

E_U (Mpsi)	R	$\Delta\alpha/R$ (ppm/ºC)
0.9	5.04	0.83
1.4	6.64	0.63
2.0	8.42	0.50

As E_U increases, the underfill layer provides increased coupling between the chip and substrate and the strain reduction factor increases from 5.04 to 8.42. The solder joints see an effective CTE mismatch under 1 ppm/ºC, over four times less than the CTE-mismatch of the assembly without underfill, $\Delta\alpha_G$ = 4.2 ppm/ºC (for silicon on alumina). Other applications of the underfill model and parametric studies are given in [8], including chip size effects and the relation between maximum interfacial stresses in the underfill layer and delamination failures.

MODEL IMPLEMENTATION

Input Parameters

Accurate acquisition, reporting and saving of assembly reliability data (geometric parameters, material properties, test results) is essential for the interpretation of test results and for field reliability assessment. Handbook values can be used for standard material properties (e.g.: silicon). Measurements are necessary for product specific materials and constructions (e.g. in-plane expansivities of organic boards or component CTEs). This makes data gathering a significant part of the reliability evaluation process. Model development and interpretation of published reliability data have suffered from a lack of standardized formatting of test information as accelerated test results are reported with varying degrees of completeness. Sometimes, test information and material properties are available by direct communication with authors of reliability reports and material suppliers. In other cases, the information is unavailable because of the purpose of the experiment (e.g.: A to B comparison) or the proprietary nature of the data.

The SRS design-for-reliability tool includes a standard PC-based filing system for electronic saving of input data and analysis results. Such a system enables the easy exchange of project information for reliability assessment under a variety of application-specific use conditions. The file-keeper(s) of an organization can build-up and maintain a library of assembly reliability data for reference or use in future applications. This aspect of assembly reliability programs is important as evidenced by the development of in-house databases for model development and verification [2, 3, 7, 9, 28].

Input parameters for reliability evaluation using SRS and assembly stiffness models are listed below. Component mechanical drawings, solder joint cross-sections are essential information as well. Lead geometry and material properties are needed for leaded assemblies stiffness calculations. Also needed for PBGA analysis are the material properties and thickness of internal layers, plus pad thickness and properties for the attachment copper pads.

- Component data:
  - ◊ Distance to Neutral Point (in)
  - ◊ Component thickness (in)
  - ◊ Effective in-plane component CTE (/ºC)
  - ◊ Effective Young's modulus in tension (psi) (for global mismatch)
  - ◊ Effective Young's modulus in flexure (psi) (for global mismatch)
  - ◊ Thickness of lead or component at solder joint (in)
  - ◊ Effective CTE of lead or component at solder joint (/ºC) (for local mismatch)
  - ◊ Effective Young's modulus of lead material or component (psi) (for local mismatch)

- Substrate data:
  - ◊ Effective in-plane CTE in diagonal direction of component (/ºC) (determined from X and Y in-plane CTEs and component aspect ratio)
  - ◊ Effective Young's modulus (psi) in tension
  - ◊ Effective Young's modulus (psi) in flexure
  - ◊ Thickness

- Assembly data:
  - ◊ Assembly stiffness (lb/in)
  (diagonal lead stiffness for leaded assemblies or combined stretching and bending stiffness of parts for leadless assemblies)
  - ◊ Solder joint effective thickness or component stand-off (in) (half the solder paste thickness for leaded assemblies)
  - ◊ Solder joint load bearing area / crack area (in^2)

- Reliability parameters:
  - ◊ Number of susceptible I/Os
  - ◊ Slope of 2P Weibull distribution
  - ◊ Ratio of failure free time to characteristic life for 3P Weibull analysis.
  - ◊ Intended design life (years)

- Thermal conditions (for multiple thermal loads):

	T_{HOT} (°C)	T_{COLD} (°C)	Hot Dwell (min.)	Cold dwell (min.)	Fixed cycle count (cycles)	Frequency of variable cycles (cycles/day)
Cond. 1						
Cond. 2						
etc...						

Note: fixed cycles are cycles that occur at the beginning of the product life (e.g.: EST, shipping, storage...). Variable cycles occur throughout the product life at an estimated frequency in cycles/day (e.g.: season-dependent environmental cycles for outdoor equipment; usage cycles: on/off cycles, mini-cycles, etc...).

Life Predictions

Life predictions for a product application with multiple thermal conditions are derived from Miner's rule [44]. The applicability of Miner's rule to solder joint thermal fatigue has been demonstrated by R. Darveaux [45] using TSOP accelerated test results. Miner's rule, whose theoretical basis is that cyclic strain energy accumulates in metals up to a critical value when failure occurs, is consistent with energy-based solder joint fatigue models.

Using 2P Weibull failure statistics for the distribution of solder joint failures, the number of years in the field, N_{YEARS}, when a fraction F of the component population has failed is obtained by setting Miner's cumulative damage equal to 1 and solving equation (38) for N_{YEARS}:

$$\left(\frac{n_1}{N_1(F)}+\frac{n_2}{N_2(F)}+\ldots\right)+365.25\cdot N_{YEARS}\left(\frac{f_A}{N_A(F)}+\frac{f_B}{N_B(F)}+\ldots\right)=1 \quad (38)$$

where:

- n_i is the number of accumulated cycles for one time occurrence, "fixed" thermal loads (index i = 1, 2...), e.g.: EST, shipping, storage cycles.
- f_i is the daily cyclic frequency (in cycles/day) for "variable" thermal loads (index i = A, B...) that occur throughout the product life.
- $N_i(F)$ are cycles to a fraction failed of F for each thermal condition i = 1,2... and i = A, B... For each individual thermal load, $N_i(F)$ is obtained as:

$$N_i(F)=\alpha_i\left[-\ln(1-F)\right]^{1/\beta} \quad (39)$$

where α_i, the component characteristic life for condition i, is calculated by the SRS model.

Inversely, equations (38) and (39) can be solved for F to determine the fraction failed at a given number of years in the field.

Using three-parameter (3P) Weibull failure statistics [9], the number of failure-free years in the field is obtained by solving Miner's rule equation for $N_{0,YEARS}$:

$$\left(\frac{n_1}{N_{0,1}}+\frac{n_2}{N_{0,2}}+\ldots\right)+365.25\cdot N_{0,YEARS}\left(\frac{f_A}{N_{0,A}}+\frac{f_B}{N_{0,B}}+\ldots\right)=1 \quad (40)$$

where $N_{0,i}$ are failure free cycles for each thermal condition i = 1,2... and i = A, B... At the present time, the SRS model does not have a correlation of failure-free time test data available to predict the $N_{0,i}$'s directly. Instead, the PC-based design-for-reliability tool uses a parameter "r" defined as the ratio of failure free time to characteristic life to predict failure free times from the correlation of characteristic lives. When test data are available, the parameter r can be adjusted so the failure free time prediction matches the failure-free time from 3P Weibull analysis of test failures. The parameter r has been observed in the range 0.21 to 0.73 [2, 9] and an average value of 0.5 is used in Darveaux's model [2].

Design-For-Reliability Tool / Performance Evaluation

The SRS model has been implemented as a PC-based design-for-reliability tool which streamlines the assembly reliability assessment process. The tool consists of:

- A pre-processor for input of component, substrate, assembly, thermal profiles, design life and statistical parameters, and component-specific stiffness and CTE calculations.

- An analysis module to compute hysteresis loops.
- A post-processor to examine stress/strain plots and life prediction results.

Once geometric parameters and material properties have been gathered, data input takes a few minutes and hysteresis loop computations take seconds on a low-end personal computer. The classical mechanics approach in SRS offers significant savings in CPU time over finite-element models with run times of one to twenty four hours per thermal condition on workstations.

The finite element method remains a powerful tool in the hands of analysts with expertise in the use of high-end non-linear FEA codes, mesh size and time-step definition, stress singularity and numerical convergence problems. In a recent study, R. Darveaux [5] reported differences of two to three times in the scaling constants of crack initiation and crack propagation correlations when using 0.3 mil or 2.0 mil element sizes. Other recommendations for FEA modeling of solder joints [5] included using elements of consistent size across a database of assembly models, and volume-averaging of strain energy results for interface elements as opposed to using singularity-sensitive nodal values at edges of solder joints.

The SRS model does not have the geometric detailing capabilities of finite-element models. However, the model is thought to be conceptually clear and is intended to capture main effects. Its validation by a wide range of accelerated tests and strain measurement techniques, and its implementation on low end personal computers make it a practical, fast turnaround design tool.

CONCLUSIONS

A solder joint fatigue model, SRS, has been developed using the classical engineering mechanics approach to capture the main effects of solder joint deformations and joint interaction with the attached component and substrate. The model has been validated by thirty three accelerated tests and several strain measurement experiments. SRS has been implemented as a PC-based design-for-reliability tool that applies to the grand families of surface mount components from LCCCs to leaded assemblies, area-array and emerging chip-scale packages. Model improvements and extension to new technologies are underway and will be reported in future publications.

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REFERENCES

[1] D. Noctor, F. E. Bader, A. P. Viera, P. Boysan, S. Golwalkar and R. Foehringer, “Solder joint attachment reliability evaluation and failure analysis of thin small outline packages (TSOPs) with alloy 42 leads”, IEEE Trans. on CHMT, Vol. 16, No. 8, December 1993, pp. 961-971.

[2] R. Darveaux, K. Banerji, A. Mawer and G. Dody, "Reliability of plastic ball grid array assemblies", Chap. 13, *Ball Grid Array Technology*, ed. J. H. Lau, McGraw-Hill, 1995, pp. 379-442.

[3] Z. Mei, "TSOP solder joint reliability", Proceedings, 46th ECTC, Orlando, FL, May 28-31, 1996, pp. 1232-1238.

[4] P. Zarrow and D. Kopp, “Component technology: decisions and issues”, Circuits Assemblies, June 1996, pp. 24-25.

[5] R. Darveaux, “How to use finite element analysis to predict solder joint fatigue life”, Proceedings, VIII International Congress on Experimental Mechanics, Nashville, TN, June 10-13, 1996, pp. 41-42.

[6] J-P. Clech, "Solder Reliability Solutions: from LCCCs to area array assemblies", Proceedings, Nepcon West '96, pp. 1665-1680.

[7] J-P. Clech, J. C. Manock, D. M. Noctor, F. E. Bader and J. A. Augis, "A Comprehensive Surface Mount Reliability model covering several generations of packaging and assembly technology", IEEE Trans. on CHMT, vol. 16, No. 8, December 1993, pp. 949-960.

[8] J-P. Clech, “Strength and reliability of flip chip assemblies with underfill”, submitted for publication.

[9] J-P. Clech, D. M. Noctor, J. C. Manock, G. W. Lynott and F. E. Bader, “Surface mount failure statistics and failure free time”, Proceedings, 44th ECTC, Washington, DC, May 1-4, 1994, pp. 487-497.

[10] R. Darveaux, "Crack initiation and growth in surface mount solder joints," Proceedings, ISHM Conference, November 9-11, 1993, Dallas, TX, pp. 86-97.

[11] W. M. Sherry and P. M. Hall, “Materials, structures, and mechanics of solder joints for surface mount microelectronics technology”, Proceedings, Interconnection Technology in Electronics, Fellbach, Germany, Feb. 1988, pp. 47-61.

[12] W. Engelmaier, “Surface mount attachment reliability of clip-leaded ceramic chip carriers on FR-4 circuit boards”, IEEE Trans. on CHMT, vol. 12, No. 2, June 1989, pp. 284-296.

[13] L. L. Hines, “SOT-23 surface mount attachment reliability studies”, Proceedings, IEPS, Boston, MA, Nov. 1987, pp. 613-629.

[14] J. H. Lau, Y-H. Pao, C. Larner, R. Govila, S. Twerefour, D. Gilbert, S. Erasmus and S. Dolot, “Reliability of 0.4 mm pitch, 256-pin Plastic Quad Flat pack no-clean and water-clean solder joints”, Soldering

and Surface Mount Technology, No. 16, February 1994, pp. 42-50.

[15] J. Lau, S. Golwalkar, P. Boysan, R. Surratt, R. Forhinger and S. Erasmus, "Solder joint reliability of a Thin Small Outline Package (TSOP)", Circuit World, Vol. 20, No. 1, 1993, pp. 12-19.

[16] P. M. Hall, "Creep and stress relaxation in solder joints", Chapter 10, *Solder Joint Reliability: Theory and Applications*, ed. J. H. Lau, Van Nostrand Reinhold, 1991, pp. 306-332.

[17] J-P. Clech and J. A. Augis, "Temperature cycling, structural response and attachment reliability of surface mounted leaded packages", Proceedings, IEPS, Dallas, TX, Nov. 7-10, 1988, pp. 305-325.

[18] R. W. Kotlowitz, "Comparative compliance of generic lead designs for surface mounted components", Proceedings, IEPS, Boston, MA, Nov. 9-11, 1987, Vol. 2, pp. 965-984.

[19] R. W. Kotlowitz, "Compliance metrics for surface mount component lead design", Proceedings, ECTC, Las Vegas, NV, May 21-23, 1990, pp. 1054-1063.

[20] S. Knecht and L. Fox, "Integrated matrix creep: application to accelerated testing and lifetime prediction", Chapter 16, *Solder Joint Reliability: Theory and Applications*, ed. J. H. Lau, Van Nostrand Reinhold, 1991, pp. 508-544.

[21] M. C. Shine and L. R. Fox, "Fatigue of solder joints in surface mount devices", Low Cycle Fatigue, ASTM STP 942, 1988, pp. 588-610.

[22] B. Wong, D. E. Helling and R. W. Clark, "A creep rupture model for two-phase eutectic solders", IEEE CHMT Trans., vol. II, No. 3, Sept. 1988, pp. 284-290.

[23] D. Stone, S. Hanula and C-Y. Li, "The effects of service and material variables on the fatigue behavior of solder joints during the thermal cycles", Proceedings, 1985 Electronic Components Conference, pp. 46-51.

[24] R. Darveaux and K. Banerji, "Constitutive relations for tin-based solder joints", Proceedings, 42nd ECTC, San Diego, CA, May 1992, pp. 538-551.

[25] P. M. Hall, "Forces, moments, and displacements during thermal chamber cycling of leadless ceramic chip carriers soldered to printed boards", IEEE Trans. on CHMT, 1984, Vol. 7, No. 4, Dec. 1994, pp. 314-327.

[26] E. Jih and Y-H. Pao, "Evaluation of design parameters for leadless chip resistors solder joints", J. of Electronic Packaging, ASME Trans., Vol. 117, No. 2, June 1995, pp. 94-99.

[27] J-P. Clech, F. M. Langerman and J. A. Augis, "Local CTE mismatch in SM leaded packages: a potential reliability concern," Proceedings, 40th ECTC, Las Vegas, Nevada, May 21-23, 1990, pp. 368-376.

[28] L. C. Wen, G. R. Mon and R. G. Ross, Jr., "Reliability Assessment of Solder Joints on LCCC Packages", in *Summary of the Phase 1 Round Robin Solder Joint Life Prediction Model Results*, ed. K. Bonner and S. Cornford, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, October 28, 1994.

[29] L. C. Wen and R. G. Ross, Jr., "Comparison of LCC solder joint life predictions with experimental data", ASME Trans., Journal of Electronic Packaging, Vol. 117, No. 2, June 1995, pp. 109-115.

[30] L. C. Wen, G. R. Mon and R. G. Ross, Jr., *Guidelines for Solder Joint Reliability Determination*, JPL D-13412, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA, June 1996.

[31] D. Noctor and J-P. Clech, "Accelerated testing and predictive modeling of the attachment reliability of alloy 42 and copper leaded TSOPs", Proceedings, Nepcon East, Boston, MA, June 14-17, 1993, pp. 193-206.

[32] R. Darveaux and A. Mawer, "Thermal and Power Cycling Limits of Plastic Ball Grid Array (PBGA) Assemblies", Proceedings, Surface Mount International '95, August 29-31, 1995, San Jose, CA, pp. 315-326.

[33] T. I. Ejim, A. Holliday, F. E. Bader and S. Gahr, "Designed Experiment to Determine Attachment Reliability Drivers for PBGA Packages", Proceedings, Surface Mount International '95, August 29-31, 1995, San Jose, CA, pp. 385-392.

[34] A. Mawer, "Ball grid array interconnect technology", presented at IPC BGA National Symposium, San Diego, January 18-19, 1996.

[35] T. I. Ejim and J-P. Clech, "Moiré analysis and modeling of area array assemblies," Proceedings, VIII International Congress on Experimental and Applied Mechanics, Nashville, TN, June 10-12, 1996, pp. 53-54.

[36] P. M. Hall, "Thermal Expansivity and Thermal Stress in Multilayered Structures", Chapter 2, *Thermal Stress and Strain in Microelectronics Packaging*, ed. J. H. Lau, Van Nostrand Reinhold, NY, 1993, pp. 78-94.

[37] T. I. Ejim, J-P. Clech, T. D. Dudderar, Y. Guo and B. Han, "Measurement of thermomechanical deformations of plastic ball grid array assemblies using moiré interferometry", Proceeding of the 1995 SEM (Society for Experimental Mechanics) Conference and Exhibit, Grand Rapids, MI, June 12-14, 1995, pp. 121-125.

[38] R. F. Gibson, *Principles of Composite Material Mechanics*, McGraw-Hill, NY, 1994.

[39] A. Blake, *Practical Stress Analysis in Engineering Design*, M. Dekker, NY, 1982.

[40] J-P. Clech, micro-BGA model, paper in preparation.

[41] J. Fjelstad and M. Perry, "Finite element analysis of a compliant chip scale ball grid array package", Proceedings, CHIPCON, February 1996.

[42] E. Suhir, "Thermal Stress Failures in Microelectronic Components - Review and Extension", Vol. 1, Chapter 5, in *Advances in Thermal Modeling of Electronic Components and Systems*, ed. A. Bar-Cohen and A. D. Kraus, Hemisphere Publishing Co., 1990, pp. 337-412.

[43] B. Han, Y. Guo and C. K. Lim "Application of

interferometric techniques to verification of numerical models for microelectronics packaging design", Advances in Electronic Packaging, InterPack '95, Maui, Hawaii, March 26-30, 1995, ASME, EEP-Vol. 10-2, pp 1187-1194.

[44] M. A. Miner, "Cumulative fatigue damage", Journal of Applied Mechanics, September 1945, pp. A-159 - A-184.

[45] R. Darveaux, "Optimizing the reliability of Thin Small Outline Package (TSOP) solder joints", Advances in Electronic Packaging, InterPack '95, Maui, Hawaii, March 26-30, 1995, ASME, EEP-Vol. 10-2, pp. 675-685.