

**TWO-DAY COURSE DESCRIPTION**

**"SMT SOLDER JOINT RELIABILITY"**

by Dr. Jean-Paul Clech, EPSI Inc., Montclair, NJ, USA  
tel.: (973)746-3796, e-mail: jpclech@aol.com

**OBJECTIVES OF THIS COURSE:**

This course presents detailed, state-of-the-art information on the solder joint reliability of conventional SMT packages and assemblies. Practical guidelines are presented to design and manufacture reliable assemblies, identify limiting factors and assess reliability under application-specific conditions. The course reviews the fundamentals of solder joint fatigue, critical parameters that influence attachment reliability for common families of leadless, leaded, BGA, flip chip and CSP components. Test data from across the industry are used to explain the impact of package construction, die size, pad design, solder volume, materials and board properties on long-term attachment reliability. Design-for-reliability tools and test methods are reviewed that enable a rapid assessment of the effect of main parameters on assembly reliability. Lessons and principles learned from SnPb reliability studies, in particular with respect to design guidelines and board to component interaction, apply equally well to lead-free assemblies.

**WHAT YOU WILL LEARN:**

- What are the key reliability issues associated with conventional SMT, BGA, flip-chip and CSP assemblies.
- What are the end-user requirements. Solder joint reliability trends and industry perspectives.
- What are the critical component and board variables that affect solder joint reliability.
- How do boards and components interact.
- How to develop effective test plans and select appropriate models to prove-in product assembly reliability.
- What are the standard test procedures, where is the reliability data.
- How to evaluate whether a particular assembly can survive your customer target design life.

The class notes distill years of industry experience and the most recent reliability data for BGA flip-chip and CSP assemblies in a single source of information that will be useful to participants long after completion of the course. Material includes presentation slides and over 300 pages of background documentation on SMT reliability, technical notes, unpublished tricks-of-the-trade and a comprehensive list of references and internet resources. Documentation includes five preview chapters from the book "SMT Solder Joint Reliability" being written by the instructor.

**PARTIAL LIST OF TOPICS**

- Assembly reliability trends, BGA / CSP reliability risks & design margins: what are the problems and how to avoid them.
- What do customers want? End-user reliability requirements; IPC test standards.
- Where is the data? Lessons learned from conventional SMT and area array assembly technology.
- Solder properties; solder joint mechanics, creep, thermo-mechanical fatigue.
- Main effects: global and local CTE mismatch problems; impact of die / package / assembly parameters; small joint size effects and the improved fatigue resistance of micro-solder joints.
- Methods for establishing assembly reliability: test procedures (thermal & mechanical cycling), modeling techniques (analytical models, Finite Element Analysis); life predictions models: under thermal cycling or vibration loads.
- Reliability of leaded assemblies; lead stiffness, package CTE; fine-pitch assemblies, reliability data.

- Reliability of BGA assemblies: die size, solder volume, pad size and pad design effects; effect of substrate thickness; 1.5 mm to 1 mm pitch BGA reliability, full vs. perimeter arrays, plastic vs. ceramic BGA; comparison to QFP attachment reliability.
- Flip-chip assembly reliability: delamination risks; underfill properties requirements.
- Solder joint reliability of low profile fine-pitch BGAs; importance of die size effects.
- CSP assemblies: reliability trends and data; importance of CSP CTEs.
- Micro-BGA assembly reliability: compliancy/decoupling mechanism; elastomer and chip size effects; effect of pad design (SMD vs. NSMD), reliability data, modeling.
- CSPs with rigid or flex interposer: fine-pitch flip-chip BGA, ceramic CSPs; reliability data, correlation of accelerated test results.
- Reliability of SON/BLP packages, ceramic/plastic CSPs & Wafer Level Package (WLP) assemblies.
- Techniques for solder joint reliability enhancements; PWB issues; lead-free solders.
- Lead-free reliability: overview, lead-free vs. SnPb reliability...

### **INSTRUCTOR'S BIOGRAPHY**

Jean-Paul Clech has 20 years of practical experience in SMT design, soldering quality and reliability assurance. He maintains one of the largest databases of solder joint reliability data, material properties and life prediction models in the industry and is constantly challenged by problems brought about by new and emerging technologies. His current research interests are in BGA, CSP, flip-chip and lead-free assembly reliability, including the development of lead-free solder acceleration factors and life prediction models.

Jean-Paul is the founder of EPSI Inc. in Montclair, NJ. His responsibilities include technical consultation and problem solving for clients across the electronics industry worldwide, and the development of engineering tools and training programs to prevent or solve reliability problems in electronic packages and board assemblies. He is the principal developer of the "Solder Reliability Solutions" model and application software. He has also served as an expert-witness in product litigations involving solder joint field failures.

Jean-Paul previously was Manager of Electronic Packaging at a European super-computer start-up, a Member of the Technical Staff and then consultant at AT&T Bell Laboratories. He received the Diplôme d' Ingénieur from Ecole Centrale de Paris, France (Materials Science major), and the M.S. and Ph.D. degrees in Mechanical Engineering from Northwestern University, Evanston, IL. His technical interests include thermal, mechanical, structural and fatigue behavior of electronic materials, packages and assemblies, and the application of engineering principles to the physical design and manufacturing of electronic systems. He is the author of over forty technical papers, a frequent speaker at technical conferences, and has been an invited lecturer and instructor at various corporate events and professional venues in Asia, Europe and North America. He is an active member of ASME, IEEE, IMAPS, TMS and SMTA. In 2003, Jean-Paul received the SMTA Member of Distinction award.

### **CONTACT INFORMATION**

Jean-Paul Clech, EPSI Inc., P.O. Box 1522, Montclair, NJ 07042, USA  
 tel: +1 (973)746-3796, fax: +1 (973)655-0815, e-mail: [jpclech@aol.com](mailto:jpclech@aol.com)  
 URL: <http://www.jpclench.com>

### **IN-HOUSE WORKSHOP**

This workshop is also available in-house at a site of your choice. When offered in-house, the .pdf version of presentation files and related documentation are available on a CD-ROM with a license agreement for posting on your company web site.