

# ACCELERATION FACTORS AND THERMAL CYCLING TEST EFFICIENCY FOR LEAD-FREE SN-AG-CU ASSEMBLIES

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## ABSTRACT

This paper reports on the development and application of a SAC thermal cycling solder joint reliability model. The strain-energy based model is used to study the effect of ramp rates, mean temperature, dwell times and temperature profile (sine vs. trapeze-like cycle) on SAC solder joint life. The model captures dwell time effects accurately. A detailed study of dwell time and ramp rate effects shows how accelerated thermal cycling profiles can be optimized to improve test efficiency. Other application examples illustrate the impact of component parameters - global mismatch in Coefficients of Thermal Expansion (CTEs) and maximum Distance to Neutral Point (DNP) - on acceleration factors.

Key words: Lead-free solder joint reliability, SAC life prediction model, dwell time, mean temperature, ramp rate effects, acceleration factors and their component dependency.

## INTRODUCTION

Statements are often made to the effect that lead-free solders are more (or less) reliable than standard SnPb solder. These general statements are incomplete when the lead-free alloy composition is not specified and when product information and use conditions are left out of the equation. Reliability being defined as the ability of a product to survive field conditions for a specified period of time, the reliability assessment of lead-free assemblies calls for quantitative estimates of solder joint lives under relevant use conditions. This assessment can be performed in one of two ways: 1) by making absolute life predictions using an established predictive model; 2) by extrapolating accelerated test results to field conditions using an appropriate Acceleration Factor (AF). While accelerated testing provides raw failure data for model calibration and/or validation, the reliability assessment of lead-free board assemblies is not complete until the above assessment has been performed.

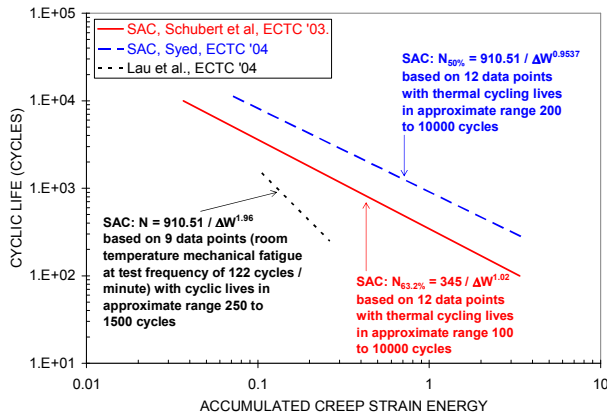
AFs are defined as the ratio of cycles to failure in the field to cycles to failure in test. Cycles to failure used in AF calculations are estimated upfront - prior to testing and

product deployment - using a life prediction model. The reason for this is that very few organizations, if any, can afford to wait for field returns to validate predictions of cycles to failure under field conditions. A variety of solder joint life prediction techniques has been available for decades for SnPb assemblies. However, model development for lead-free assemblies is relatively recent. While the author is not aware of any life prediction capability for SnBi soldered assemblies, at least a dozen different models - including the one presented in this paper - have been developed in the last two years for the more popular SnAgCu solder alloys [1-11]. The models are analytical, one-dimensional strain-energy based (as in the present paper), and strain or strain-energy based Finite-Element (FE) models. Examples of application and validation of the FE-based methodology in [9] are given in [12, 13]. Advantages and disadvantages of each model need to be weighed in carefully based on their scope of application, accuracy, cost of analysis, and speed of execution. For example, FE-based life predictions, which are typically carried by skilled analysts, take from a couple of hours to one day of computational time on a workstation, whereas algebraic or one-dimensional model execute almost instantaneously on standard computing equipment. FE models also require special consideration of element size effects since stresses and strain energy keep rising as the FE mesh is refined at the edge of solder joint interfaces. On the other hand, the FE approach is the most appropriate method when subtle geometric or material details (e. g, solder joint voids, intermetallics) need to be included in the analysis.

This paper presents work in progress on a one-dimensional, strain energy model for SAC soldered assemblies. In its present stage of development, the model only handles shear stresses and strains that arise in solder joints due to the global thermal expansion mismatch between surface mount circuit boards and components. A similar capability has been developed to account for the contribution of local CTE mismatches in to the total (local + global) cyclic strain energy. This latter part of the model is still undergoing validation and will be reported on in a future publication. As such, the present model applies only to leadless components with a

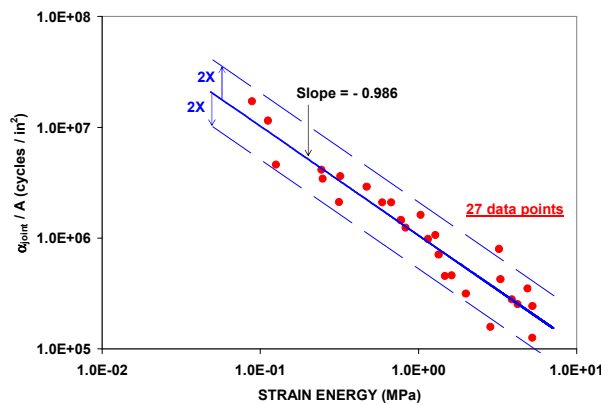
small contribution of local CTE mismatches to cyclic strain energy.

### STRAIN-ENERGY BASED MODELS



**Figure 1:** Life vs. strain energy correlations from [5, 9, 10] for SAC assemblies.

Figure 1 is a plot of three independent correlations of cyclic lives versus strain energy [5, 9, 10] for SAC solder joints of composition near that of SAC387 and SAC396 alloys (3.8-3.9% wt. Ag, 0.6-0.7% wt. Cu). The two correlations of thermal cycling data [9, 10] are each based on 12 data points that cover almost two orders of magnitude on the life and strain energy axis. Their slopes are close to  $-1$ . The correlation of isothermal (room temperature) mechanical fatigue data [5] is based on 9 data points over less than one order of magnitude in cyclic lives. The slope of this correlation is  $-1.96$ , which is in the range:  $-1/0.7 = -1.43$  to  $-1/0.5 = -2$ , given in [14] for isothermal mechanical fatigue of engineering metals.



**Figure 2:** Life / strain energy correlation for leadless SAC assemblies. Strain energy is obtained from hysteresis loops computed with one-dimensional solder joint shear strain model.

Our present correlation of SAC thermal cycling failure data, shown in Figure 2, is given as:

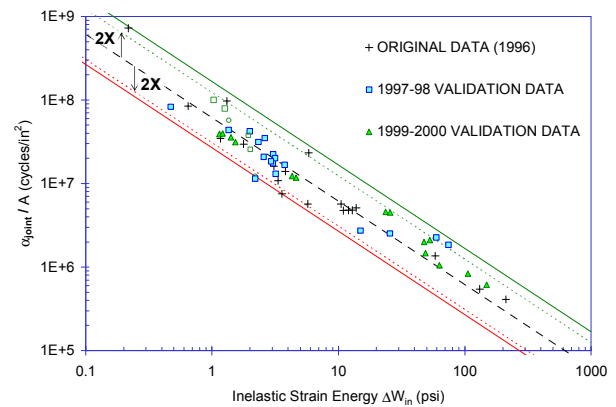
$$\frac{\alpha_{JOINT}}{A} = \frac{C}{\Delta W^m} \quad (1)$$

where  $\alpha_{JOINT}$  is the characteristic life on a per joint basis (using Weibull failure distributions from a population of critical solder joints as opposed to failure distributions for a population of components),  $A$  is the solder joint load bearing or crack area,  $C$  is a constant,  $\Delta W$  is the cyclic strain energy density obtained from the area of stress / strain hysteresis loops, and the exponent  $m$  is close to  $1$  ( $m = 0.986$ ). The 27 data points in Figure 2 cover about two orders of magnitude in each direction and the slope of the centerline correlation is close to  $-1$ . The spread of the data around the centerline is a factor of two times, which is typical of fatigue correlations.

The slopes of the three correlations of SAC thermal cycling data in Figures 1 and 2 are consistent and close to  $-1$  in spite of the fact that the three models use different constitutive models for SAC solder. We thus hypothesize that, under thermal cycling conditions, SAC cycles to failure go as the inverse of cyclic strain energies. A similar, theoretical relationship was first proposed for thermal cycling of soft solders [15] based on the application of dislocation theory to generic solder fatigue damage models. An inverse relationship between thermal cycling life and strain energy was also arrived at in [16] using a combination of fracture mechanics theory, Miner's rule cumulative damage and a Monkman-Grant creep rupture criterion. AFs are thus obtained as the ratio of cyclic strain energies ( $\Delta W$ ) under test and field conditions:

$$AF \equiv \frac{N_f(field)}{N_f(test)} = \frac{\Delta W(test)}{\Delta W(field)} \quad (2)$$

where the  $N_f$ 's are cycles to failure and the  $\Delta W$ 's are cyclic strain energies under test and field conditions.



**Figure 3:** Life vs. strain energy correlation of the SRS model for standard SnPb assemblies [17-19].

For comparison purposes, Figure 3 shows the life / strain energy correlation (as in equation (1)) developed for SnPb assemblies using the Solder Reliability Solutions (SRS) model [17-19]. The slope of the correlation of SnPb thermal cycling failure data is  $-0.998$ , based on the initial correlation of training data from 19 experiments. The set of training plus validation data shown in Figure 3 covers two and a half orders of magnitude along both axis. It is

thus reasonable to set a goal for SAC reliability models to cover from two to three orders of magnitude along both the life and strain energy axis.

### SHEAR STRESS AND STRAIN MODEL

The shear stress and strain model that is used to compute hysteresis loops follows the exact same procedures that were developed for the SRS model [17-19] except that temperature ramp rates are included in the present analysis. Ramp rates are accounted for by performing a step-by-step integration of creep rate equations along the prescribed temperature profile. The method applies to any temperature profile. Examples of thermal cycling hysteresis loops for sine and trapeze-like temperature profiles will be shown later for illustration purposes.

The present model captures elastic and creep deformations of both SnPb and SAC solders. One simplification of the model is that the creep constitutive equation only includes minimum creep rates, using equations (7) and (15) in [20] for creep of Sn37Pb and Sn3.8Ag0.7Cu solders, respectively. The minimum creep rate law for SnPb was shown to follow hysteresis loop measurements closely for a ceramic chip carrier on FR4 (Figure 7 in [20]). The creep rate formulation for SAC was shown to predict the shear strength of SAC solder joints in chip scale assemblies at 25°C, 75°C and 125°C (Figure 25 in [20]). In the future, we plan to upgrade the current methodology using a more advanced constitutive model that accounts for both primary and tertiary creep of solders [21].

Emphasis in the rest of this paper is on applications and validation of the model in order to better quantify and understand the response of SAC solder joints under thermal cycling conditions. This includes studies of the dwell times, ramp rates and mean temperature effects on solder joint lives of both SnPb and SAC assemblies. Implications in terms of thermal cycling test efficiency for SAC assemblies are also discussed. Examples of SAC AFs are given, that illustrate the impact of board and component parameters on AFs.

### DWELL TIME EFFECTS

#### HOT DWELL EFFECT: SHORT VS. LONG

In this section, we study the effect of changing the dwell time on the hot side of a temperature profile alone. Figure 4 shows hysteresis loops at outermost corner joints under the die (17 mm x 17 mm x 0.33 mm) of a 1 mm pitch, 676 I/O Plastic Ball Grid Array (PBGA) on a 2.36 mm (93 mil) thick FR-4 board with Organic Solderability Preservative (OSP) finish. The stress/strain simulations are for a SAC test vehicle assembled and thermally cycled by a consortium of companies known as the Industry Working Group (IWG) [22]. The BGA ball and solder paste alloys were Sn4.0Ag0.5Cu and Sn3.9Ag0.5Cu, respectively. The peak reflow temperature was 235°C.

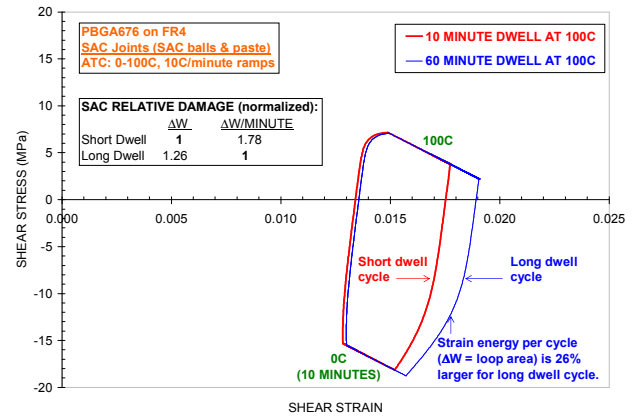


Figure 4: Hysteresis loops of SAC outermost corner joints under die shadow in 676 I/O PBGA on FR-4.

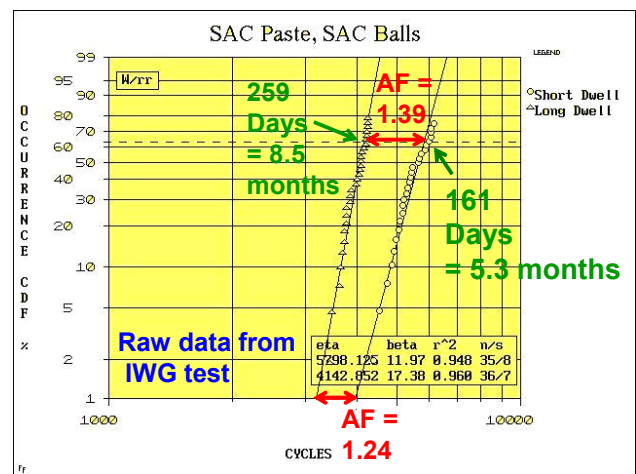


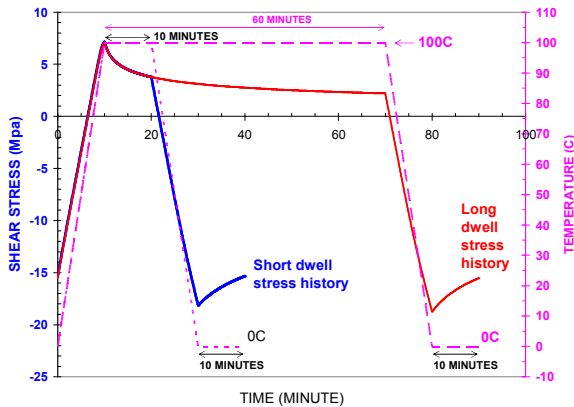
Figure 5: 2P Weibull plot of failure cycles for SAC PBGA assemblies subject to ATC (0/100°C) with short (10 minutes) and long dwell (60 minutes) times at 100°C.

	AF	AF Calculation Method
MODEL	1.26	Predicted as ratio of hysteresis loop areas in Figure 4.
TEST	1.24	Calculated as ratio of cycles to 1% failure in test (2P Weibull)
	1.39	Calculated as ratio of cycles to 63.2% failure in test (2P Weibull).
	1.288	Calculated as ratio of failure-free cycles in test (3P Weibull).
Test Average	1.306	Average of above three AFs in test.

Table 1: Comparison of predicted and experimental AFs for SAC PBGA676 assemblies.

Accelerated Thermal Cycling (ATC) was between 0°C and 100°C with 10 minute ramps, a 10 minute cold dwell and 10 (“short”) or 60 (“long”) minute hot dwell. Test frequencies are 16 and 36 cycles/day, respectively, for the “long” and “short” dwell test profiles. The reader is referred to [22] for further details on the test vehicle, test conditions and failure analysis results. Figure 5 shows the distribution of failure cycles for the two test profiles

on two-parameter (2P) Weibull paper. Using three-parameter (3P) Weibull distributions, failure free cycles in test were obtained as:  $N_{0,Short\ Dwell} = 3963$  cycles and  $N_{0,Long\ Dwell} = 3077$  cycles for the “short” and “long” hot dwell cycles, respectively (see Figure 22 in [22]). The ratio of loop areas in Figure 4 is 1.26, i.e., the predicted AF between the two test conditions is 1.26. The comparison of predicted and experimental AF in Table 1 indicates that the average experimental AF of 1.306 is 3.7% higher than the predicted AF of 1.26.

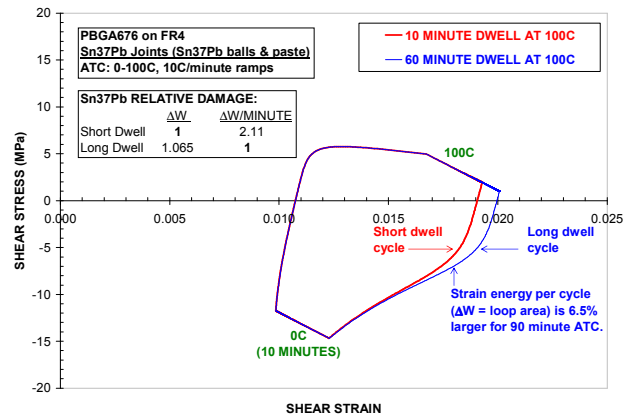


**Figure 6:** Stress and temperature histories for SAC PBGA assemblies under “short” and “long” dwell ATC.

The temperature and stress histories along the hysteresis loops in Figure 4 are plotted in Figure 6. Stress relaxation proceeds at the fastest rate at the beginning of dwell periods (cold and hot). At 100°C, 50% stress reduction is achieved in the first ten minutes. Stress reduction slows down as time goes on and it takes another fifty minutes to reach 74% stress reduction at the end of the “long” dwell at 100°C. On the cold side, the percentage of stress reduction at the end of the 10 minute cold dwell is about the same (15 to 17%) for the two temperature profiles. In terms of damage rate, defined as cyclic strain energy per unit of time (or loop area over cycle duration), that of the “short” dwell cycle is 1.78 times larger than that of the “long” dwell cycle. That is, the “short” dwell cycle is more efficient at creating creep-fatigue damage in the SAC solder joints than the “long” dwell cycle. Given that failure modes and mechanisms are similar in the two tests [22], and that the predicted AF is in excellent agreement with the experimental AF, the results of the two accelerated test profiles are consistent with each other. The whole experiment [22] and the hysteresis loop analysis lead to the conclusion that the “long” dwell time at 100°C is not necessary for the PBGA assembly of interest.

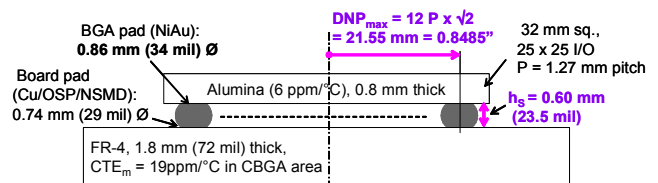
For comparison purposes, Figure 7 shows the equivalent Sn37Pb hysteresis loops for a similar (non-tested) assembly with SnPb instead of SAC solder joints. Here, the difference in loop areas is smaller (ratio of 1.06 times) than in the SAC case. Because of more rapid stress reduction at 100°C, “longer” dwells on the hot side of the cycle are even more inefficient than in the case of SAC

assemblies. The damage rate for the “short” dwell cycle is twice as much as for the “long” dwell cycle. A more important difference between the SAC and SnPb hysteresis loops is that the stress ranges are quite different, with typically higher stresses in SAC than in SnPb assemblies: ~ 7 MPa (SAC) vs. ~ 5 MPa (SnPb) on the hot side of the cycle, and -18 MPa (SAC) vs. -14.5 MPa (SnPb) on the cold side of the cycle. The SAC solder joints build up higher stresses during the temperature ramps and experience entirely different stress histories than SnPb joints throughout a given thermal cycle. It is thus erroneous to design accelerated temperature profiles by simply comparing creep rates for the two alloys since creep rates come from isothermal creep tests conducted under constant load (or stress).



**Figure 7:** Hysteresis loops of Sn37Pb outermost corner joints under die shadow in 676 I/O PBGA on FR-4.

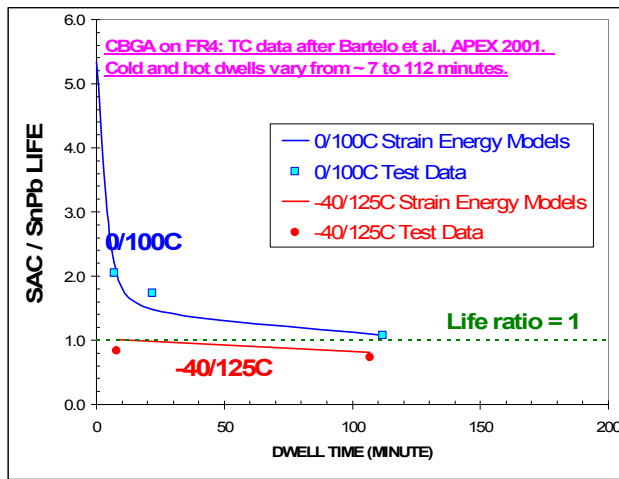
### EQUAL DWELL TIMES: SHORT VS. LONG



**Figure 8:** Basic test vehicle geometry and material properties for 32 x 32 mm sq. Ceramic BGA (CBGA).

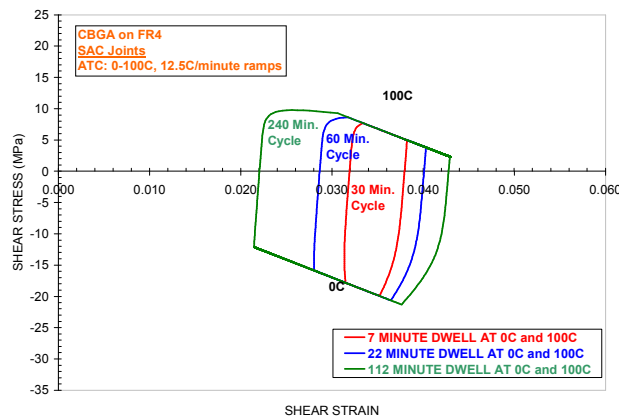
This section investigates the effect of changing the hot and cold dwell times equally for SAC387 and standard SnPb assemblies. Experimental data [23] is for CBGA assemblies which were tested under ATC conditions with equal hot and cold dwell times of about 7, 22 and 112 minutes. Using an average ramp rate of about 12.5°C/minute in stress/strain loop simulations, the corresponding cycle lengths are 30, 60 and 240 minutes for thermal cycling between 0°C and 100°C, with respective test frequencies of 48, 24 and 6 cycles/day (CPD). Basic geometry and material properties were gathered from [23]. A summary description of the test vehicle parameters used in the simulation is given in Figure 8. Young’s modulus for alumina was taken as  $E = 37$  Mpsi, that of the standard type of FR-4 was assigned a typical value of 2.5 Mpsi. Since log-normal failure distributions in [23] were normalized for each

temperature profile, the goal of the present simulation is only to predict the effect of dwell times on the ratio of SAC to SnPb median lives, as shown in Figure 9.

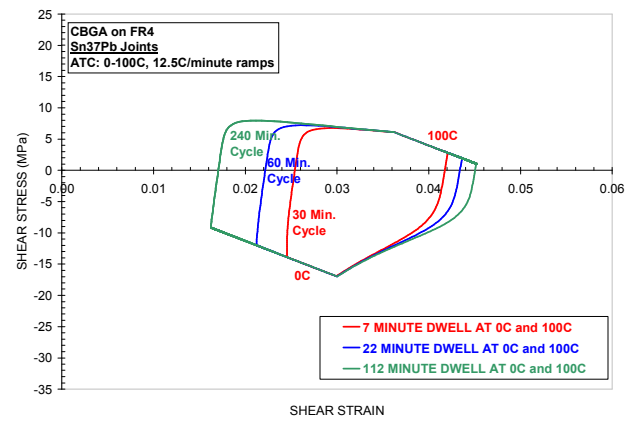


**Figure 9:** Predicted and experimental trends of SAC to SnPb median life ratio as a function of dwell time in Thermal Cycling (TC). CBGA data points are from normalized failure distributions in [23].

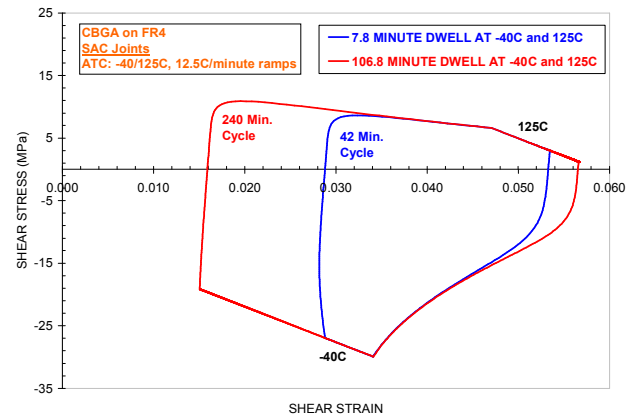
Model trends (solid lines in Figure 9) for the ratio of median lives vs. dwell times follow the experimental results closely. Under 0/100°C conditions, the life ratio is greater than 1 for dwell times up to about 112 minutes. However, extrapolation of the model trend suggests that the life ratio would be less than 1 for longer dwells. Under harsher -40/125°C conditions, the life ratio is less than 1, even at short dwell times. This does not mean that the SAC solder joints are unreliable or less reliable than SnPb solder joints. Since the strain energy models predict the effect of dwell times correctly, the model can be used to extrapolate test results for any of the above dwell times to make an estimate of life under use of conditions of interest. It is only after extrapolation to use conditions that one can conclude whether life requirements are met (or not) for both SnPb and SAC assemblies. This extrapolation exercise could not be completed in the context of this particular simulation since absolute cycles to failure were not available in [23].



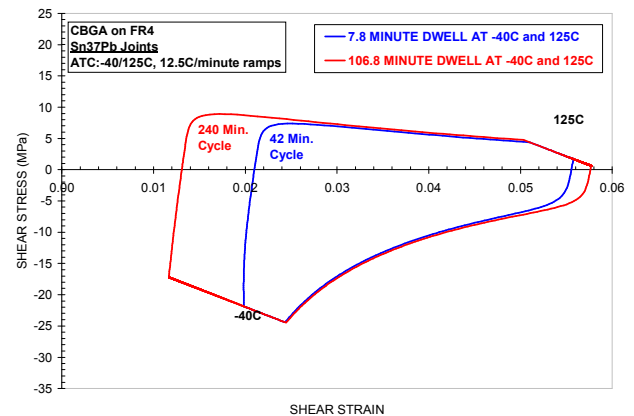
(a) SAC, 0/100°C



(b) SnPb, 0/100°C



(c) SAC, -40/125°C



(d) SnPb, -40/125°C

**Figure 10:** Hysteresis loops for SAC and SnPb CBGA solder joints under thermal conditions: a) and b): 0/100°C; c) and d): -40/125°C.

0/100C	CYCLE LENGTH (MINUTES)	30	60	240
	$\Delta W$ (normalized)	1.00	1.92	3.41
-40/125C	CYCLE LENGTH (MINUTES)	42	240	
	$\Delta W$ (normalized)	4.65	8.09	

(a) Strain energy per cycle, normalized for 0/100°C, 30 minute cycle length condition.

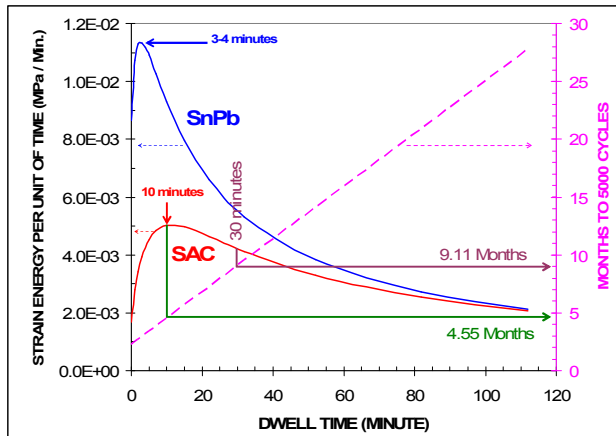
0/100C	CYCLE LENGTH (MINUTES)	30	60	240
	$\Delta W$ / Unit of Time (normalized)	1.00	0.96	0.43
-40/125C	CYCLE LENGTH (MINUTES)	42	240	
	$\Delta W$ / Unit of Time (normalized)	3.32	1.01	

(b) Damage rate (strain energy per unit of time), normalized for 0/100°C, 30 minute cycle length condition.

**Table 2:** Strain energy per cycle and damage rate for the SAC hysteresis loops in Figure 10.

Hysteresis loops for the SnPb and SAC CBGA solder joints of interest are shown on the same scale in Figures 10a-d. In all cases, SAC joints build up higher stresses than SnPb joints during the ramps, which, as in the case of 676 I/O PBGA assemblies, confirms that SAC and SnPb solder joints experience different stress histories. The SAC strain energy results and damage rates for all five thermal conditions are given in Table 2 where results are normalized with respect to the 0/100°C, 30 minute cycle length condition. This gives a relative comparison of loop areas (Table 2a), and more importantly, an indication of test efficiency (Table 2b). For 0/100°C ATC, the 30 minute cycle (~ 7 min. dwells) and the 60 minute cycle (~22 min. dwells) have about the same damage rate (1 vs. 0.96). The damage rate of the long dwell cycle (0/100°C, 240 min. length, 112 min. dwells) is  $1/0.43 = 2.3$  times less than for the short dwell cycle. As in the previous PBGA study, the above observations do not indicate any benefit to a 0/100°C ATC test with long dwell times. Overall, the most efficient of the five temperature profiles is the -40/125°C, 40 min. length, 7 min. dwell test profile. Its damage rate is 3.32 times that of the 0/100°C, 7 min. dwell test.

### OPTIMUM DWELL TIME



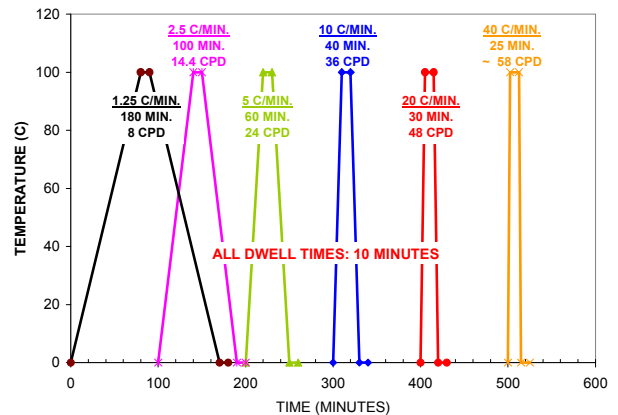
**Figure 11:** Damage rate or strain energy per unit of time (solid lines, primary axis) and test duration given as months to 5000 cycles (dashed line, secondary axis) as a function of dwell time for SAC and SnPb CBGA assemblies in thermal cycling from 0°C to 100°C.

Having validated the SAC strain energy model for dwell time effects, simulations were run to look for an optimum dwell time. This was done for the same SnPb and SAC CBGA assemblies as in the previous section and for thermal cycling between 0°C and 100°C (12.5°C/min. ramps). Results are shown as damage rate or strain energy per unit of time ( $\Delta W$  / Cycle Length) versus dwell time (equal dwells at 0°C and 100°C) in Figure 11. Dwell times of 10 and 3 to 4 minutes give the maximum damage rate for SAC and SnPb assemblies, respectively. The optimum dwell time for SAC is about three times longer than the optimum dwell time for standard SnPb. Looking at the corresponding test duration on the secondary vertical axis in Figure 11, a 10 minute dwell time for SAC assemblies leads to 4.5 months of testing to reach 5000 cycles. A 30 minute dwell time gives about 9.1 months of testing to reach the same 5000 cycle count.

The SAC strain energy model correlates thermal cycling data from multiple experiments (Figure 2) using different component types and test conditions. The application of the model to the study of dwell time effects in SAC assemblies - including validation of the model for dwell periods in the range 7 to 112 minutes - suggests that extended dwell times are not necessary under typical ATC conditions. Although it may not be near optimum test conditions, the use of long dwell times is technically valid and may be economically acceptable for organizations with adequate time and resources to conduct extended test programs.

### RAMP RATE EFFECTS

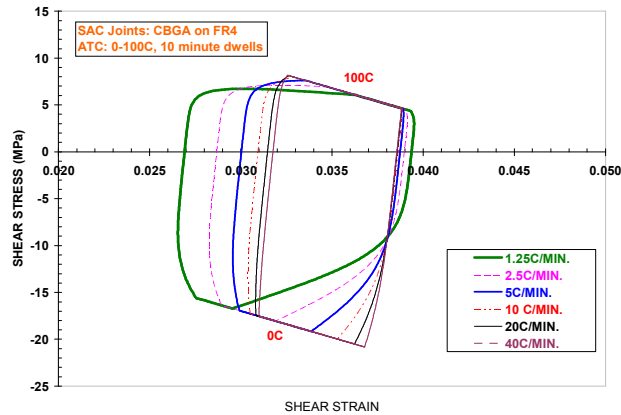
#### STRESS/STRAIN ANALYSIS



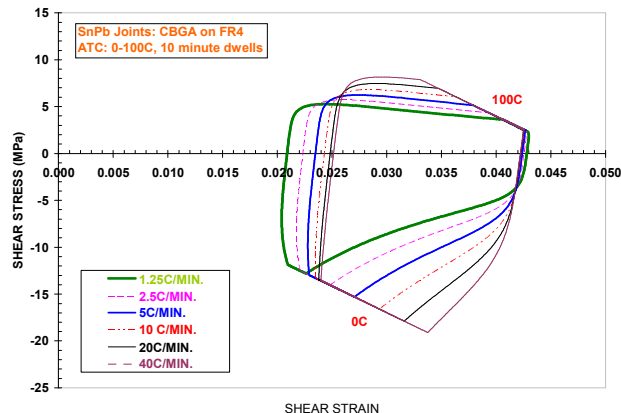
**Figure 12:** Temperature profiles used in ramp rate study. Ramp rate labels are followed by cycle length (in minutes) and test frequency (in Cycles/Day or CPD).

Cycle length and test duration are also affected by ramp rates. In order to investigate the effect of ramp rates on both SAC and SnPb solder joint lives, the previous CBGA and PBGA models were run under conditions: 0/100°C, 10 minute dwells (cold and hot) and with ramp rates

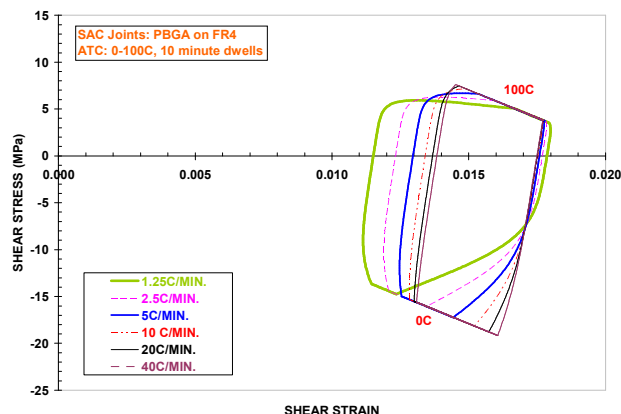
(equal rates up and down) in the range 1.25°C/minute to 40°C/minute. The simulations were run for six temperature profiles - shown in Figure 12 - with ramp rates being doubled from one profile to the next. These profiles have test frequencies from 8 CPD (slowest ramp at 1.25°C/min.) to about 58 CPD (fastest ramp at 40°C/min.). Hysteresis loops are plotted in Figures 13a to 13d. For both SAC and SnPb assemblies, higher stresses build up during temperature ramps when the ramp rate increases. The cyclic strain range increases and a larger fraction of it is developed during the ramps as the temperature ramp rate decreases.



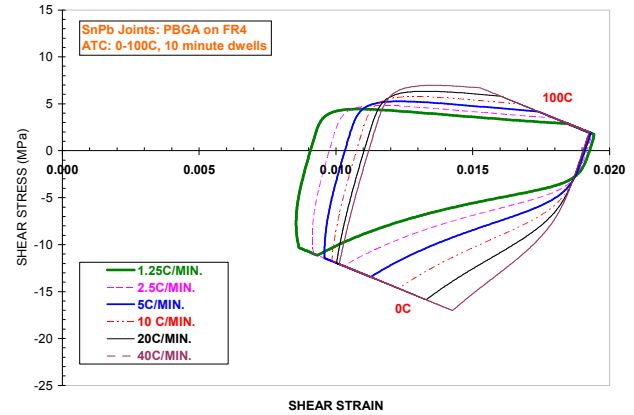
(a) SAC CBGA



(b) SnPb CBGA



(c) SAC PBGA



(d) SnPb CBGA

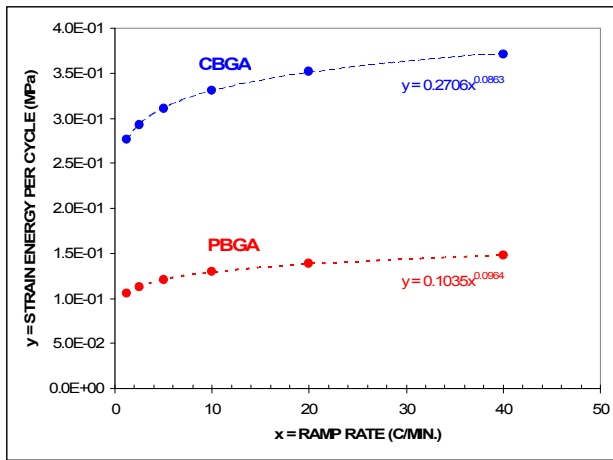
**Figure 13:** SAC and SnPb CBGA / PBGA hysteresis loops for different ramp rates in thermal cycling between 0°C and 100°C with 10 minute dwells (cold and hot).

### RAMP RATE RESULTS

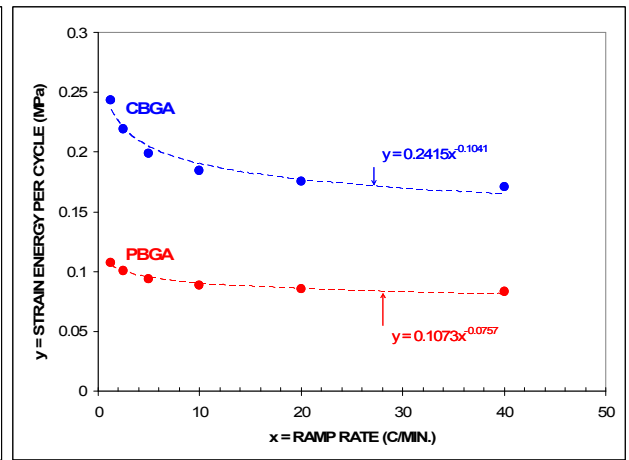
Ramp rate strain energy and cyclic life results are shown in Figures 14 and 15 for SnPb and SAC assemblies, respectively. Cyclic strain energy results as a function of ramp rates in Figures 14a (SnPb) and 15a (SAC) are fitted with power-law trendlines. For the two alloys, the power-law exponents are small with absolute values in the range 0.075 to 0.104. This suggests a weak dependence of cyclic strain energy on ramp rates. The cyclic strain energy results in Figures 14a and 15a are re-plotted as relative cyclic lives vs. ramp rates in Figures 14b and 15b. For each package and alloy, cyclic lives are normalized with respect to the predicted life for the 10°C/minute ramp rate condition.

While the effect of ramp rates on cyclic lives is weak (with power-law exponents that are exactly opposite those of the strain energy trendlines in Figures 14a and 15a), an apparently surprising fact is that the ramp rate effect goes in opposite directions for SnPb and SAC. This is consistent with other modeling and experimental data:

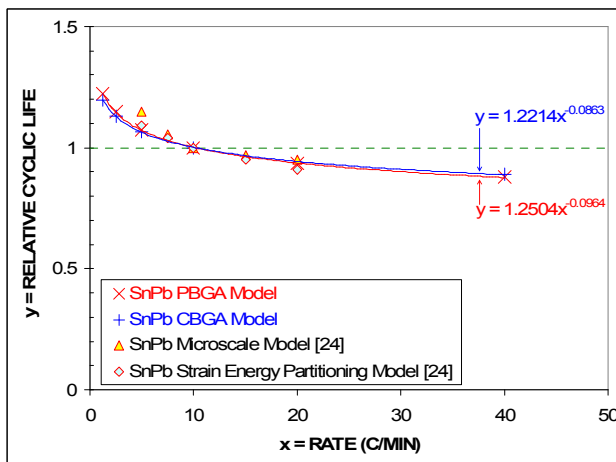
- The weak dependence of SnPb cyclic lives on ramp rates is supported by accelerated test results in [24]. ATC failure data in [24] indicates that there was no statistical difference in the characteristic lives of SnPb assemblies (using nine different package types) tested between 0°C and 100°C at ramp rates of 10 and 20°C/minute. Failure modes were also identical, namely, bulk solder fatigue. We are not aware of a similar experiment having been conducted for SAC assemblies. Further experimentation is recommended to check on the weak dependence of SAC cyclic lives on ramp rates.
- About SnPb lives that decrease with ramp rates: we have added two sets of data points in Figure 14b from two separate analysis of the effect of ramp rates on



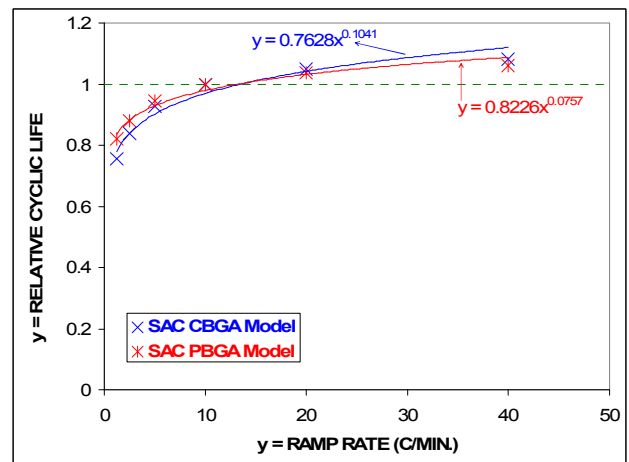
(a) SnPb cyclic strain energy vs. ramp rate.



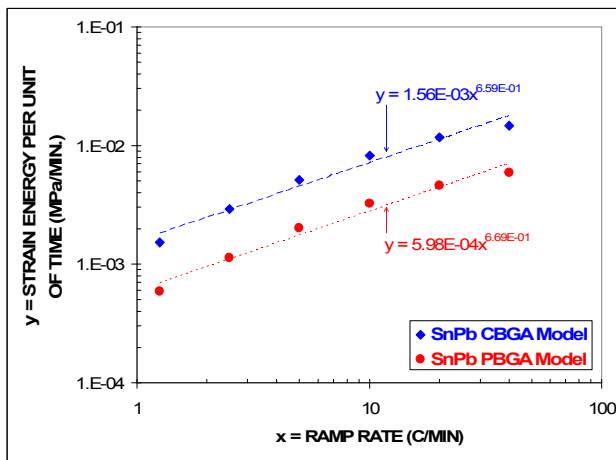
(a) SAC cyclic strain energy vs. ramp rate.



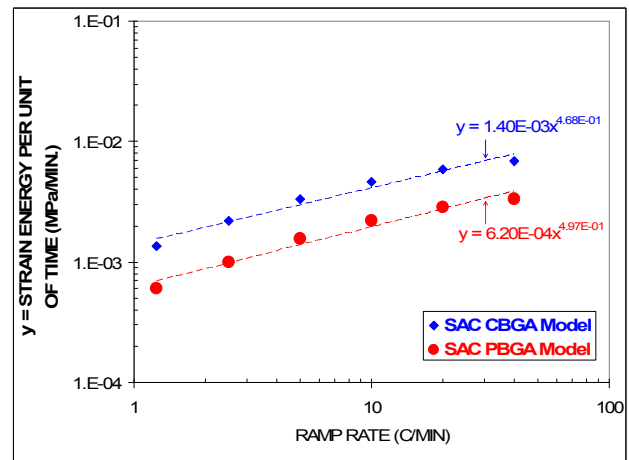
(b) SnPb relative cyclic life vs. ramp rate.



(b) SAC relative cyclic life vs. ramp rate.



(c) SnPb strain energy per unit of time vs. ramp rate.



(c) SAC strain energy per unit of time vs. ramp rate.

**Figure 14:** “Ramp rate” strain energy results for SnPb PBGA and CBGA assemblies.

**Figure 15:** “Ramp rate” strain energy results for SAC PBGA and CBGA assemblies.



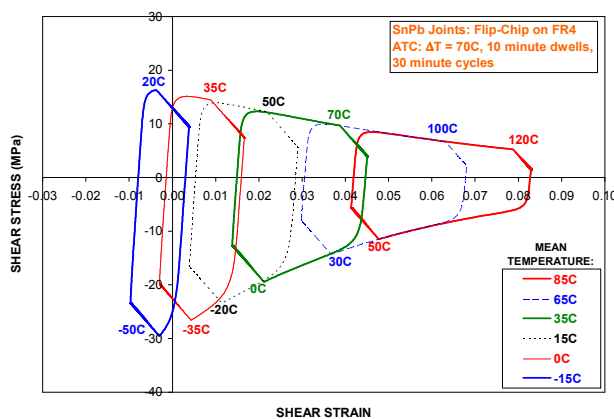
the cyclic lives of SnPb assemblies [25]. SnPb predictions from these two different modeling techniques [25] follow our own SnPb CBGA and PBGA model trends closely. That is, three different SnPb models predict that SnPb cyclic lives decrease with increasing ramp rates.

- About SAC lives that increase with ramp rates: thermal cycling failure distributions are not available yet (to this author's knowledge) to test the validity of the predicted trend in Figure 15b directly. However, a study of ramp rate effects on the shear strength of SAC chip resistor solder joints [26] concluded that thermal cycling with the slowest ramp rate (10°C/minute) lead to the largest reduction in shear strength after 1200 ATC cycles. In comparison, much less strength reduction was observed after thermal cycling with higher ramp rates (up to 55°C/minute). Strength measurements lead to the conclusion that slower ramps create more damage per cycle (not per unit of time) for SAC solder joints in chip resistor assemblies. This is in agreement with the predicted trend of cyclic strain energy increasing with slower ramp rates in Figure 15a.

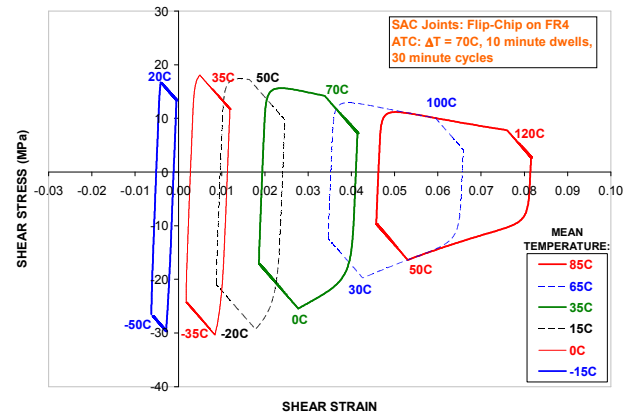
Although cyclic strain energy has a weak dependence on ramp rates, the damage rate or strain energy per unit of time (not per cycle) increases rapidly with ramp rates as seen in Figures 14c and 15c. Power-law trendlines fitted through the model data points in Figures 14c and 15c have average exponents of 0.66 (~ 2/3) for SnPb assemblies and 0.48 (almost a square root dependence) for SAC assemblies. Provided that bulk solder fatigue remains the dominant failure mode, faster ramps provide a further opportunity to reduce test duration. This was verified experimentally in [24] for SnPb assemblies under thermal cycling with ramp rates in the range 10 to 20°C/minute.

## MEAN TEMPERATURE EFFECTS

### STRESS / STRAIN ANALYSIS



(a) SnPb loops.



(b) SAC loops

**Figure 16:** SnPb and SAC solder joints hysteresis loops for increasing mean temperature (fixed  $\Delta T = 70^\circ\text{C}$ , 30 minute cycle, 10 minute dwells).

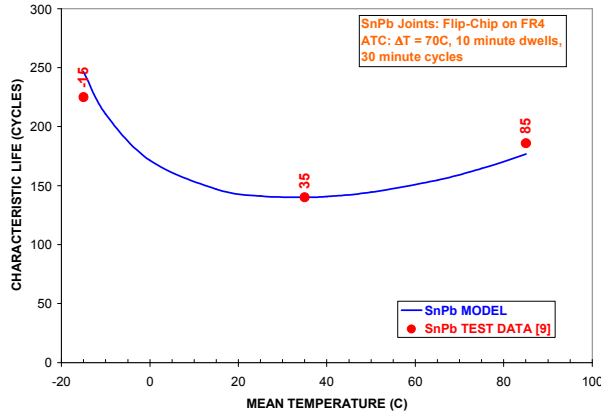
Figures 16a and 16b show SnPb and SAC solder joint hysteresis loops for the outermost corner joints of non-underfilled flip-chip assemblies on FR-4. Loops are shown for a thermal cycle with a fixed temperature swing ( $\Delta T = 70^\circ\text{C}$ , 30 minute cycle, 10 minute dwells) and mean temperatures varying from  $-15^\circ\text{C}$  to  $85^\circ\text{C}$ . The model simulates a flip-chip test vehicle and experiment [9] with solder joint characteristic lives available for three thermal profiles:  $-50^\circ\text{C}$  to  $20^\circ\text{C}$  (mean temperature =  $-15^\circ\text{C}$ ),  $0^\circ\text{C}$  to  $70^\circ\text{C}$  (mean =  $35^\circ\text{C}$ ) and  $50^\circ\text{C}$  to  $120^\circ\text{C}$  (mean =  $85^\circ\text{C}$ ).

The general trend displayed by SnPb and SAC hysteresis loops is that, as the mean temperature goes up, the strain range (loop width) increases while the stress range (loop height) decreases. Since the strain and stress ranges evolve in opposite directions, the loop area will be maximum for some intermediate value of mean temperature. At that point, solder joint life will be minimum and will increase with further increases in mean temperature. This has significant implications as discussed in the following sections.

### MEAN TEMPERATURE RESULTS: SN-PB

SnPb test data from [9] are plotted as characteristic life versus mean temperature in Figure 17. While the raw data clearly shows that solder joint life will display a minimum for some intermediate mean temperature, there is not enough experimental data to pinpoint where the minimum occurs. Reference [9] did not provide a discussion of why the test data suggests a minimum life. Based on SnPb hysteresis loop areas in Figure 16a (plus additional loops that are not shown for other values of the mean temperature), the model line (solid line) in Figure 17 indicates that the minimum life is reached for a mean temperature of about  $35^\circ\text{C}$  ( $0^\circ\text{C}$  to  $70^\circ\text{C}$  cycle). A very similar trend (not shown) was predicted for the same SnPb flip-chip assemblies using the SRS model [17-19]. Last, note that the temperature at which the minimum life occurs is expected to depend on the component, board

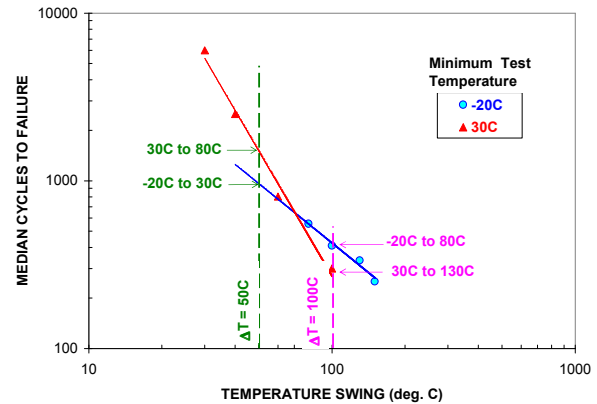
types as well as the temperature swing  $\Delta T$  and dwell times at the temperature extremes.



**Figure 17:** Mean temperature effect on flip-chip SnPb solder joint life: test data are from [9]; model line is from SnPb hysteresis loop model in this paper.

The observed minimum life from both experimental data and life predictions goes against conventional thinking which assumes that SnPb solder joint life keeps decreasing as the mean temperature rises. The main reason for the existence of a minimum life is the evolution of stress and strain ranges in opposite directions, as discussed in the previous section. Additional evidence supporting the minimum life concept is available from accelerated thermal cycling and modeling of other SnPb assemblies:

- In a talk given at ECTC 2005, authors [26] presented SnPb solder joint life data for 68 and 84 I/O Leadless Ceramic Chip Carriers (LCCCs) on FR-4 versus hot temperatures of 75°C, 100°C and 125°C for a thermal cycle with a temperature swing  $\Delta T = 100^\circ\text{C}$ . The corresponding mean temperatures are 25°C, 50°C and 75°C, respectively. Thermal cycles were run with dwell times of 15 and 75 minutes. For each combination of component size and dwell time (i.e., four independent datasets), the plot of characteristic life versus maximum temperature clearly showed that lives for a hot temperature of 125°C (mean = 75°C) was similar to or longer than the lives for a maximum temperature of 100°C (mean = 50°C). The relevant data is not in the paper [26] and the presenters did not discuss why the life vs. maximum temperature displayed a minimum.
- Figure 18 shows failure data from [27] for 84 I/O SnPb LCCCs on FR4. The data points, which were read off Figure 15 in [27], are plotted as median cycles-to-failure versus the temperature change ( $\Delta T$ ) for given cold temperatures of -20°C or 30°C. Power law trendlines that are fit through the -20°C and 30°C minimum temperature datasets have a cross-over point. Mean temperature effects and life trends go in opposite directions to the left and to the right of that cross-over point.



**Figure 18:** LCCC mean solder joint life vs. temperature swing ( $\Delta T$ ) for cold temperatures of -20°C and 30°C (data points from Figure 15 in [27]).

- To the right, and for a temperature swing of 100°C as shown in Figure 18, the test data and best-fit lines give the following median cycles to failure for thermal cycles with a cold temperature of -20 or 30°C:

$\Delta T = 100^\circ\text{C}$	Fail Cycles
-20 to 80C	410
30 to 130C	300

With a lower mean temperature of 30°C, the -20 to 80°C condition gives a **longer** solder joint life than the 30 to 130°C condition with a mean temperature of 80°C. This is as expected according to Coffin-Manson type life prediction models and conventional thinking, i.e. when the mean temperature is higher, solder creeps more and solder joint life decreases. This would occur for any temperature change to the right of the cross-over point in Figure 18.

- To the left of the cross-over point, and for a 50°C temperature change as shown in Figure 18, median cycles to failure are:

$\Delta T = 50^\circ\text{C}$	Fail Cycles
-20 to 30C	938
30 to 80C	1772

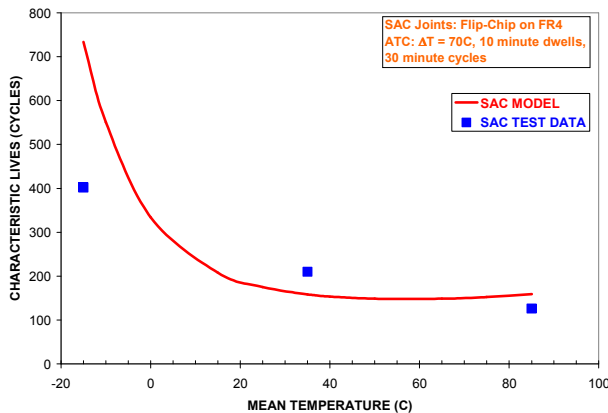
With a lower mean temperature of 5°C, the -20 to 30°C condition gives a **shorter** solder joint life than the 30 to 80°C condition with a mean temperature of 50°C. This is contrary to conventional thinking and Coffin-Manson type life prediction models. This reversal of trends would occur for any temperature changes to the left of the cross-over point. This trend, whereby colder cycles lead to shorter lives than hotter cycles, is in agreement with the previously discussed minimum life concept.

- Independent users [28] of the SRS model [17-19] have reported solder joint life predictions under

thermal cycling conditions with a fixed temperature swing where, past a certain point, cycles to failure increase when the mean temperature keeps rising.

Six experimental datasets [9, 26, 27], and at least two strain energy based life prediction models, indicate that, for a fixed temperature swing, increases in mean temperature lead to a minimum solder joint life. Beyond that point, solder joint life increases with further increases in the mean temperature. As discussed above, as well as in the previous section, strain energy models capture that characteristic of soft solders well. Coffin-Manson life prediction models, which do not account for the reduction in the maximum stress range as the mean temperature increases, do not.

**MEAN TEMPERATURE RESULTS: SAC SOLDER**



**Figure 19:** Mean temperature effect on flip-chip SAC solder joint life: test data are from [9]; model line is from SAC hysteresis loop model in this paper.

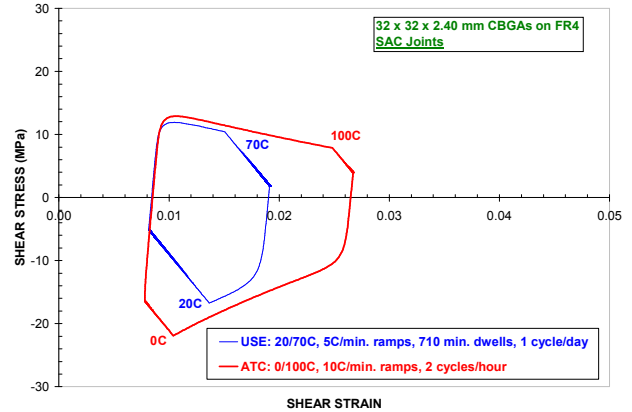
SAC test data from [9] and life predictions using the SAC hysteresis loop model are plotted as characteristic life versus mean temperature in Figure 19. The data points are scattered around the life prediction line, which is not untypical of fatigue data. The model predictions suggest a minimum life for a mean temperature somewhere in the range 50°C to 65°C. The evolution of SAC hysteresis loops with increasing mean temperature being similar to that of SnPb assemblies (see Figure 16), a minimum life is expected as well for the flip-chip SAC assemblies. However, given the apparent scatter in the data, and the small number of data points, the comparison of test and life predictions for SAC solder joints is inconclusive. Further experimentation is warranted to verify or to disprove the minimum life concept for SAC assemblies.

**ACCELERATION FACTORS**

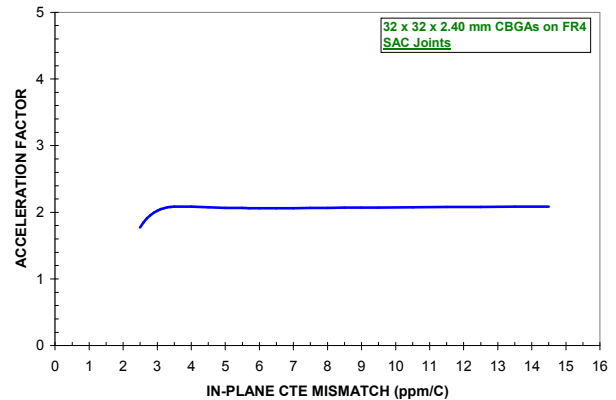
**EFFECT OF GLOBAL CTE MISMATCH ON AFs**

The first application example is that of SAC AFs for a 1 mm pitch (31 x 31 I/O array with six solder balls removed from each corner), 32 mm square, 2.40 mm thick alumina CBGA on 72 mil thick FR-4 board. The test vehicle is

modeled after a test board [2] that underwent accelerated thermal cycling between 0°C and 100°C at a test frequency of 2 Cycles Per Hour (CPH). Cycle length is 30 minute per cycle. The measured temperature profile was not available but is reasonably assumed to have approximately 10 minute ramps and 5 minute dwells, as in similar tests from the same authors’ organization. The test vehicle is as described in [2]. The SAC solder joints were 15 mil tall. Failure times [2] that were fitted to a log-normal failure distribution gave a median life  $N_{50\%} = 1310$  cycles and a standard deviation  $\sigma = 0.16$ . Most of the design information and material properties are available in [2], except for the board in-plane CTE.



**Figure 20:** SAC CBGA hysteresis loops for use (20/70°C, 1 CPD) and ATC conditions (0/100°C, 2 CPH). Loops are shown for a global CTE mismatch  $\Delta\alpha = 5.7$  ppm/°C.



**Figure 21:** CBGA acceleration factor versus global CTE mismatch for ATC conditions: 0/100°C (2 CPH) and use conditions: 20/70°C (1CPD) with a trapeze-like profile.

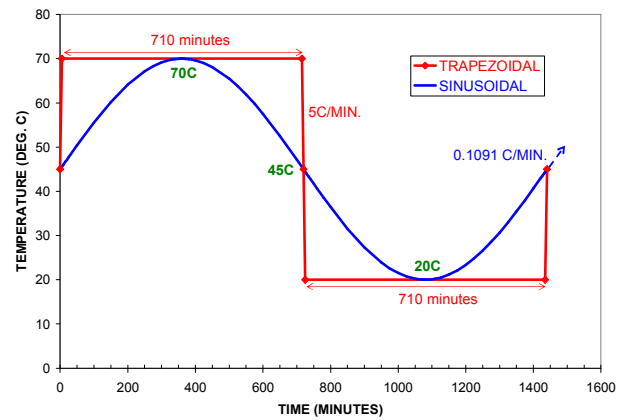
The purpose of this analysis is to investigate the impact of this unknown board CTE and, by the same token, that of the global in-plane CTE mismatch on the extrapolation of ATC test results to use conditions. For illustration purposes, hypothetical field conditions are picked as a trapeze-like daily thermal cycle with 5°C/min. ramps between 20°C and 70°C, and equal dwell times of 710 minutes on the cold and hot sides of the cycle.

Hysteresis loops for the outermost, near-corner joints were generated under use and ATC conditions for CTE

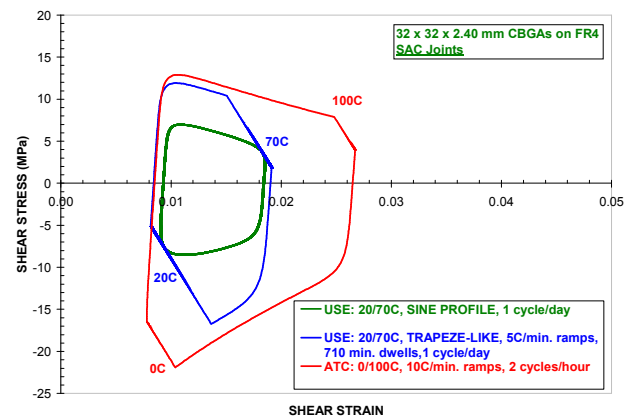
mismatches in the range 2.5 to 14.5 ppm/°C. The example loops shown in Figure 20 are for a CTE mismatch of 5.7 ppm/°C, i.e., a board CTE of 12.2 ppm/°C since the assumed CTE of the alumina CBGA substrate was taken as 6.5 ppm/°C. The AF between ATC and use conditions is calculated as the ratio of the two loop areas. This assumes that the product board assembly and the test vehicle have identical design parameters and material properties. Because the actual board CTE was not available, the loop and AF analysis were repeated for various board CTEs. Figure 21 shows the dependency of the AF on the global CTE mismatch. For mismatches in the range  $\Delta\alpha = 3.4$  to 14.5 ppm/°C, the AF is in the range 2.06 to 2.08. For smaller CTE mismatches, the AF drops. It would probably be affected by contributions of the local CTE mismatch to cyclic strain energy as well. As long as the global CTE mismatch is large enough, the AF is rather insensitive to it and to the assumed board CTE. Given that the CBGA board assemblies of interest lead to a rather low median life of 1310 cycles, it is likely that the board in-plane CTE and the board-to-component CTE mismatch were large enough that the applicable AF is in the low sensitivity area of Figure 21. For extrapolation to use conditions (see next section), we thus use an AF of 2.06. The low sensitivity of AFs to the global CTE mismatch is consistent with the Norris-Landzberg model [29] for high-lead (95-97% wt. Pb) SnPb solder. When applied to product and test board with identical geometries and properties, the global CTE mismatch drops out of the Norris-Landzberg AF calculations. The low sensitivity of AFs to the global CTE mismatch in the SAC CBGA example in this section suggests that simplified, algebraic AF models for leadless SAC assemblies may not need to include a global CTE mismatch factor. That is, while absolute life predictions depend strongly on the global CTE mismatch, the latter may possibly be ignored in algebraic AF models that would be used to extrapolate accelerated test results from a given test vehicle to a product board assembly of similar geometry and with identical board and component material properties. Under such conditions, algebraic AF formula would likely be determined by temperature profile parameters, including the mean temperature, the temperature change, different ramp rates up and down as well as different dwell times on the cold and hot sides of test and field thermal cycles.

### TRAPEZE-LIKE VS. SINE THERMAL PROFILE

In this section, we compare predicted AFs for use conditions with hypothetical trapeze-like and sine profiles. The latter type of profile is representative of diurnal / solar type thermal loading as may be encountered, for example, in some automotive, outside plant or space applications. The simulated test vehicle is the same CBGA on FR-4 as in the previous section.



**Figure 22:** Trapeze-like and sine profile for field thermal cycles between 20°C and 70°C.

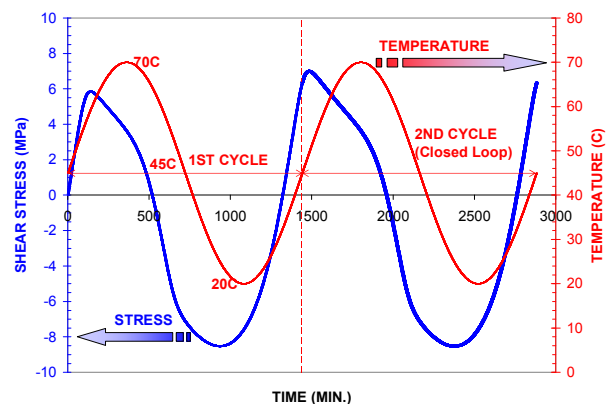


**Figure 23:** CBGA solder joint hysteresis loops under ATC conditions (0/100°C) and field cycles (20/70°C) with trapeze-like and sine temperature profiles.

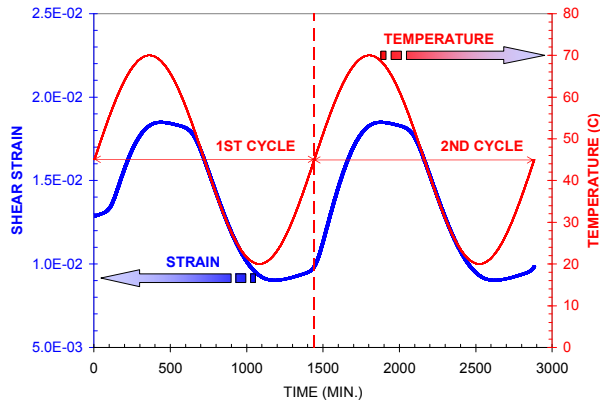
Figure 22 shows both profiles for thermal cycling between 20°C and 70°C at a use frequency of 1 CPD. The trapeze-like field profile is the same as before and the sine profile follows the equation:

$$T(t) = T_{\text{MEAN}} + \frac{\Delta T}{2} \sin(2\pi \cdot f \cdot t) \quad (3)$$

where the temperature  $T(t)$  at a given time,  $t$ , is a function of the mean temperature,  $T_{\text{mean}}$  (average of maximum,  $T_{\text{max}}$ , and minimum temperature,  $T_{\text{min}}$ ), the temperature change,  $\Delta T = T_{\text{max}} - T_{\text{min}}$ , and the cyclic frequency,  $f$ .



(a) Stress history and temperature profile.

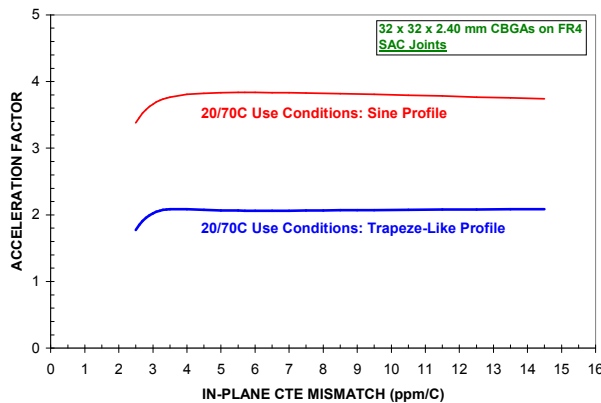


(b) Strain history and temperature profile.

**Figure 24:** Stress and strain histories for sine temperature profile (use conditions: 20/70°C, 1 CPD).

Hysteresis loops for ATC conditions, trapeze and sine temperature profiles in use are shown in Figure 23. The shown loops are for the 32 mm sq., 2.40 mm thick CBGA test vehicle with a global CTE mismatch of 5.7 ppm/°C. The area of the “sine” loop is about 1.8 times smaller than that of the loop for trapeze-like use conditions. The corresponding stress and strain histories are shown in Figure 24. The stress/strain analysis started with a zero stress condition and the loops closed (or stabilized) after just two cycles.

As in the case of a trapeze-like temperature profile, AFs for use conditions with a sine profile have a low sensitivity to CTE mismatches (same  $\Delta\alpha$  on test and product boards) that are large enough. The “sine” AF dependency on  $\Delta\alpha$  is as shown in Figure 25. For  $\Delta\alpha$  greater than 4 ppm/°C, the sine AF is in the range 3.74 to 3.84. In that area of low sensitivity, the AF for the “sine” profile is  $3.74/2.06 = 1.8$  times larger than the AF for the “trapeze-like” profile.



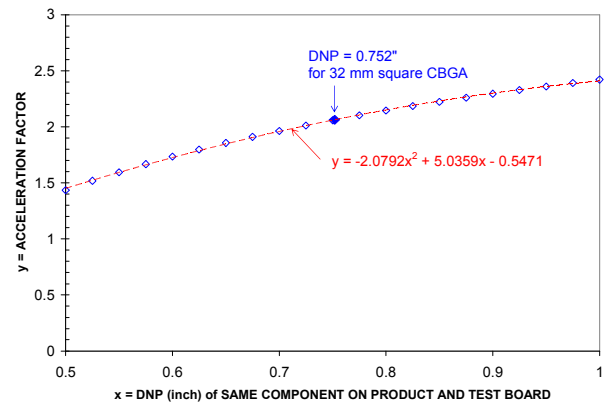
**Figure 25:** CBGA acceleration factor versus global CTE mismatch for ATC conditions: 0/100°C (2 CPH) and use conditions: 20/70°C (1CPD) with a trapeze or sine profile.

<b>N<sub>1%</sub> (ATC) (Cycles)</b>	946	
<b>N<sub>1%</sub> (Use) = N<sub>1%</sub> (Test) * AF (cycles)</b>	1949	"Trapeze-Like" Profile: AF = 2.06
	3538	"Sine" Profile: AF = 3.74
<b>Years to 1% Failure in Use =</b>	5.34	"Trapeze-Like" Profile
<b>N<sub>1%</sub> (Use) / 365.25 Cycles/Year</b>	9.69	"Sine" Profile

**Table 3:** Extrapolation of CBGA cycles to 1% failure in test to years to 1% failure in use for both trapeze-like and sine temperature profile.

Assuming the in-plane CTE of the test and product boards is large enough, the AFs are 2.06 and 3.74 for the above trapeze-like and sine temperature profiles, respectively. From the median life ( $N_{50\%} = 1310$  cycles) and the standard deviation ( $\sigma = 0.14$ ) in test [2], the log-normal failure distribution gives 946 cycles to 1% failure under ATC conditions. The life calculations in Table 3 then give a field life (years to 1% failure) of 5.3 and 9.7 years for the trapeze-like and sine temperature profiles, respectively.

### DNP EFFECT ON AFs

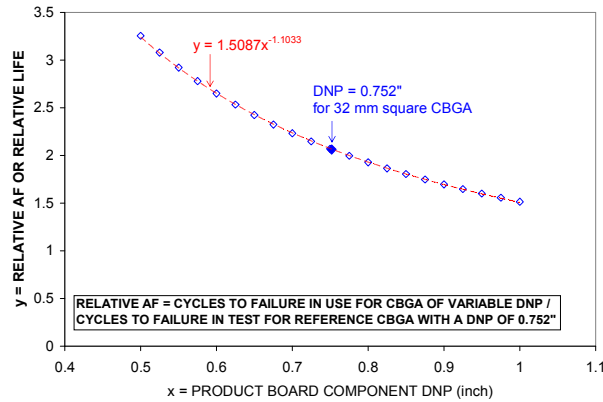


**Figure 26:** CBGA acceleration factor versus maximum DNP of identical components on product and test boards for ATC conditions: 0/100°C, 2 CPH, and use conditions: 20/70°C, 1CPD, with a trapeze-like profile.

Figure 26 shows the AF versus maximum DNP for CBGAs of different sizes (max. DNP in the range 0.5” to 1”) and for the previously defined ATC and trapeze-like use profile. AFs were calculated as before by generating hysteresis loops for variable DNPs that were identical for both the test board and the product board. The AF of 2.06 for the maximum DNP of 0.752 is for the reference test vehicle (32 mm square, 2.4 mm thick). The board-to-component CTE mismatch was maintained at 5.7 ppm/°C as in the previous reference case. The AFs increase with package size, contrary to their low sensitivity to CTE mismatches when the latter mismatches are large enough. The reason for this is that the maximum DNP affects the hysteresis loop model not only in the calculation of maximum shear strains but also in assembly stiffness calculations. Contrary to the CTE mismatch factor which can possibly be dropped out of simplified AF formulae, the DNP effect would have to be

factored in. In support of that conclusion, an experimental study of SnPb AFs [24] showed that AFs are package dependent for nine different packages of variable constructions and sizes. Power law trendlines did not fit the model data points in Figure 26. Instead, the data points are fitted with a second order polynomial.

### DNP EFFECT ON RELATIVE AFs AND LIFE

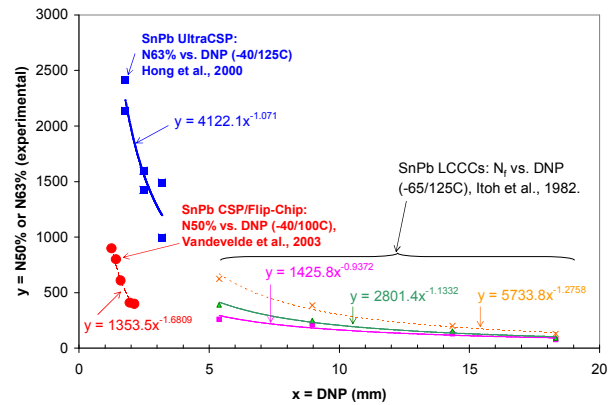


**Figure 27:** Relative AF or relative life versus maximum DNP of product board CBGA. ATC conditions are: 0/100°C, 2 CPH. Use conditions are: 20/70°C, 1 CPD, with a trapeze-like profile.

Consider a situation where the ATC failure times for the previous 32 mm square, 2.40 mm thick CBGA (maximum DNP ~ 0752”) on FR-4 are the only available test results and SAC solder joint life estimates are requested for CBGAs of other sizes, all other parameters being equal. These life estimates are obtained by using a relative AF that is defined as the ratio of cycles to failure in use for a given DNP over cycles to failure in ATC for the 32 mm square, 2.40 mm thick CBGA on FR-4. Hysteresis loops were generated for various values of the maximum DNP under trapeze-like use conditions (20/70C, 1 CPD). The relative AFs that were obtained are plotted as a function of the maximum DNP in Figure 27. These relative AFs also serve as a measure of relative solder joint life versus maximum DNP under the stated use conditions. A power-law trendline that was fitted through the model data points in Figure 27 indicates that relative AFs or relative SAC solder joint lives go as 1 / DNP<sup>1.1</sup>.

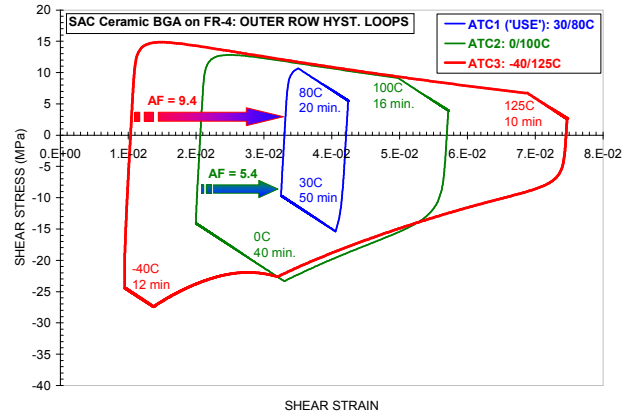
The 1.1 DNP exponent is quite different from an exponent of 1.9 for the life versus 1 / DNP relationship for high Pb solders [29] or an often quoted exponent of about 2 in Coffin-Manson reliability models for standard SnPb assemblies. However, even for standard SnPb, power-law trendlines fitted through life versus DNP data give inverse relationships with exponents that are not always near 2. For the five SnPb datasets plotted in Figure 28, the life vs. 1 / DNP relationships show exponents in the range 0.94 to 1.68. Four of the five datasets in Figure 28 give inverse power-law exponents in the range 0.94 to 1.28, and the average of these four exponents is 1.10. Including the fifth dataset with an exponent of 1.68, the

average of the five exponents is 1.22. Although we were not able to locate life versus DNP data for SAC assemblies, the 1.1 exponent in Figure 27 is consistent with the exponents obtained for the SnPb datasets in Figure 28.



**Figure 28:** Life vs. DNP experimental data [30-32] for five families of leadless components. The three LCCC datasets [30] correspond to different stand-off heights of 85, 135 and 185 μm.

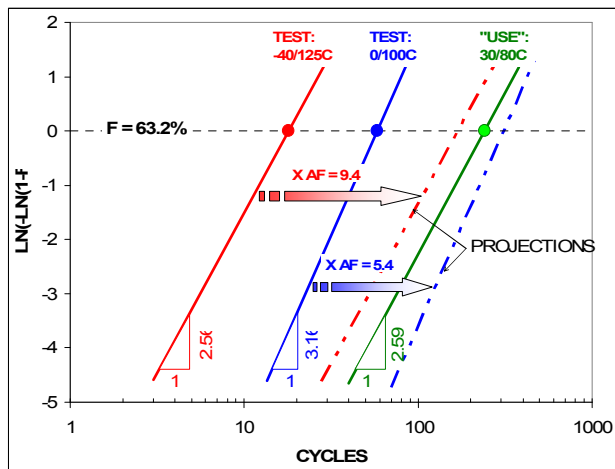
### FURTHER VALIDATION OF SAC AFs



**Figure 29:** Hysteresis loop for prototype alumina substrate on FR-4 under three ATC conditions.

Figure 29 shows hysteresis loops for the outermost corner joints of a SAC test vehicle where the component is a 30 mm square, 1 mm thick alumina substrate. The analysis is for components mounted on prototype boards as described in [8]. Test results were available for three ATC profiles: ATC1 (30/80°C), ATC2 (0/100°C) and ATC3 (-40/125°C). Temperature profiles were entered from measurements in [8]. Ramps were fairly linear except for the ATC3 condition where the ramp down part of the profile was divided into two sections to reflect a decrease in ramp down rates. This shows as a kink near the bottom side of the ATC3 loop in Figure 29. Dwell times, estimated from temperature profiles in [8], are as shown in Figure 29. In this analysis, whose purpose was to further validate the strain-energy based computation of AFs, the mildest condition ATC1 is used as a hypothetical “use” condition. From loop areas in Figure 29, the AFs

from ATC2 and ATC3 test conditions to ATC1 “use” conditions are 5.4 and 9.4, respectively.



**Figure 30:** Experimental 2P Weibull failure distributions for ATC1, ATC2 and ATC3 conditions, and projections of failure distributions from test (-40/125°C and 0/100°C) to “use” conditions (30/80°C). On vertical axis (double-log scale), F is the cumulative distribution of failures or cumulative fraction failed.

2P Weibull failure distributions for the three ATC conditions are shown as solid lines in Figure 30 using Weibull parameters - characteristic life and shape parameter - from [8]. The projections of the actual failure distributions from “test” (-40/125°C and 0/100°C) to “use” (30/80°C) conditions are obtained by translating the failure distributions in “test” by a multiplicative factor (the above calculated AFs) along the horizontal logarithmic scale. The projected failure distributions under “use” conditions are shown as semi-dashed lines in Figure 30. The projected characteristic lives are within 30% from the actual characteristic life under “use” (30/80°C) conditions. Based on this and other examples (not shown here), SAC AFs calculated with the present hysteresis loop model have a 30% uncertainty.

## CONCLUSIONS

This paper reported on work in progress on a SAC solder joint life prediction model and SAC acceleration factors. In its present condition, the strain-energy based model applies only to leadless components. An extended version that includes the effect of local CTE mismatches - an important factor for attachment reliability of leaded packages - is under development and will be reported on in the future. The present model was used to better understand the response of SAC solder assemblies under thermal cycling conditions. The life vs. strain energy correlation of the SAC model is based on 27 independent datasets. The slope of thermal cycling life vs. strain energy correlation is close to -1, consistent with that of other FEA-based strain-energy correlations. The model, which has also been validated for dwell time effects, can

be used to optimize accelerated test conditions. Examples shown in the paper illustrate the impact of dwell time, ramp rate and profile type (sine vs. trapezoidal) on solder joint life and acceleration factors. Global CTE mismatches that are large enough were found to have a weak effect on AFs. However, maximum DNP have a stronger effect which is supported by the fact that experimental AFs are package-dependent [24].

## ACKNOWLEDGEMENTS

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## REFERENCES

- [1] Che, F. X., Pang, J. H. L., Xiong, B. S., Xu, L., Low, T. H., “Lead free solder joint reliability characterization for PBGA, PQFP and TSSOP assemblies”, Proceedings, 55th Electronic Components and Technology Conference, Orlando, FL, May 31 – June 3, 2005, pp. 916-921.
- [2] Farooq, M., Goldmann, L., Martin, G., Goldsmith, C. and Bergeron, C., “Thermo-mechanical fatigue reliability of Pb-free ceramic ball grid arrays: experimental data and life time prediction modeling”, Proceedings, 53<sup>rd</sup> Electronic Components and Technology Conference, New-Orleans, LA, May 27-30, 2003.
- [3] Guédon-Gracia, A., "Contribution à l'exploitation d'un système de caractérisation thermomécanique pour la conception optimisée d'assemblage sans plomb", PhD Thesis, ENSEIRB, IXL, University of Bordeaux, France, 2005.
- [4] Lall, P., Singh, N., Strickland, M., Blanche, J. and Suhling, J., “Decision-support models for thermo-mechanical reliability of leadfree flip-chip electronics in extreme environments”, Proceedings, 55th Electronic Components and Technology Conference, Orlando, FL, May 31 – June 3, 2005, pp. 127-136.
- [5] Lau, J. H., Shangguan, D., Lau, D. C. Y., Kung, T. T. W. and Lee, S. W. R., “Thermal-fatigue life prediction equation for Wafer-Level Chip Scale (WLCSP) lead-free solder joints on lead-free Printed Circuit Board (PCB)”, Proceedings, 54<sup>th</sup> Electronic Components and Technology Conference, Las Vegas, NV, June 1-4, 2004.
- [6] Ng, H. S., Tee, T. Y., Goh, K. Y., Luan, J-E., Reinikainen, T., Husa, E. and Kujala, A., “Absolute and relative fatigue life prediction methodology for virtual qualification and design enhancement of lead-free BGA”, Proceedings, 55th Electronic Components and Technology Conference, Orlando, FL, May 31 – June 3, 2005, pp. 1282-1291.
- [7] Pan, N., Henshall, G. A., Billaut, F., Dai, S., Strum, M. J., Benedetto, E. and Rayner, J., Hewlett-Packard Company. “An Acceleration Model for Sn-Ag-Cu Solder Joint Reliability Under Various Thermal

- Cycle Conditions”, Proceedings, SMTA International Conference, Chicago, IL, September 25-29, 2005.
- [8] Salmela, O., Andersson, K., Särkkä, J. and Tammenmaa, M., “Reliability analysis of some ceramic lead-free solder attachments”, Proceedings, Pan Pacific Microelectronics Symposium, SMTA, January 25-27, 2005, Kauai, Hawaii, pp. 161-169.
- [9] Schubert, A., Dudek, R., Auerswald, E., Gollhardt, A., Michel, B. and Reichl, H., “Fatigue life models for SnAgCu and SnPb solder joints evaluated by experiments and simulation”, Proceedings, 53<sup>rd</sup> Electronic Components and Technology Conference, New-Orleans, LA, May 27-30, 2003.
- [10] Syed, A., “Accumulated creep strain energy and energy density based thermal fatigue life prediction models for SnAgCu solder joints”, Proceedings, 54<sup>th</sup> Electronic Components and Technology Conference, Las Vegas, NV, June 1-4, 2004, pp. 737-746.
- [11] Zhang, Q., Dasgupta, A. and Haswell, P., “Viscoplastic constitutive properties and energy-partitioning model of lead-free Sn3.9Ag0.6Cu solder alloy”, Proceedings, 53<sup>rd</sup> Electronic Components and Technology Conference, New-Orleans, LA, May 27-30, 2003.
- [12] Dudek, R., Döring, R., Michel, B., Picault, A. and Autissier, J.-F., “Thermo-mechanical reliability analyses on solder joints of ceramic components”, Proceedings, IPC / Soldertec Global 3<sup>rd</sup> International Conference on Lead Free Electronics, Barcelona, Spain, June 7-10, 2005.
- [13] Gonzalez, M., Vandeveld, B., Vanfleteren, J. and Manassis, D., “Thermo-mechanical FEM analysis of lead free and lead containing solder for Flip Chip applications”, Proceedings, EMPC 2005 Conference, IMAPS Europe, Bruges, Belgium, 12-15 June 2005, pp. 440-445.
- [14] Morrow, J., “Cyclic plastic strain energy and fatigue of metals”, in *Internal Friction, Damping and Cyclic Plasticity*, 67<sup>th</sup> Annual Meeting, American Society for Testing and Materials, Chicago, IL, June 22, 1964, ASTM Special Technical Publication No. 378, ASTM, Philadelphia, pp. 45-86.
- [15] Huang, J., Lai, H. Y., Qian, Y. Y. and Wang, Q. L., “A dislocation model of shear fatigue damage and life prediction of SMT solder joints under thermal cycling”, *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, Vol. 15, No. 4, August 1992, pp. 553-558.
- [16] Syed, A. R., “ACES of finite element and life prediction models for solder joint reliability”, Proceedings, *Design & Reliability of Solders and Solder Interconnections*, Symposium held during the TMS Annual Meeting, Orlando, FL, February 10-13, 1997, pp. 347-355.
- [17] Clech, J-P., "Solder Reliability Solutions: a PC-based design-for-reliability tool", Proceedings, Surface Mount International Conference, Sept. 8-12, 1996, San Jose, CA, pp. 136-151 (available for download at [www.jpcltech.com](http://www.jpcltech.com)). Republished in *Soldering and Surface Mount Technology*, Wela Publications, British Isles, Vol. 9, No. 2, July 1997, pp. 45-54.
- [18] Clech, J-P., "Flip-chip / CSP assembly reliability and solder volume effects", Proceedings, Surface Mount International Conference, San Jose, CA, August 25-27, 1998, pp. 315-324 (available for download at [www.jpcltech.com](http://www.jpcltech.com)).
- [19] Clech, J-P., "Solder joint reliability of CSP versus BGA assemblies", Proceedings, System Integration in Micro Electronics, SMT ESS & Hybrids Conference, Nuremberg, Germany, June 27-29, 2000, pp. 19-28 151 (available for download at [www.jpcltech.com](http://www.jpcltech.com)).
- [20] Clech, J-P., "An obstacle-controlled creep model for SnPb and Sn-based lead-free solders", Proceedings, SMTA International (SMTAI) Conference, Chicago, IL, Sept. 26-30, 2004, pp. 776-802 (available for download at [www.jpcltech.com](http://www.jpcltech.com)).
- [21] Clech, J-P., “An extension of the omega method to primary and tertiary creep of lead-free solders”, Proceedings, 55<sup>th</sup> Electronic Components Technology Conference (ECTC), Orlando, FL, May 31-June 3, 2005 (available for download at [www.jpcltech.com](http://www.jpcltech.com)).
- [22] Bath, J., Sethuraman, S., Zhou, X., Willie, D., Hyland, K., Newman, K., Hu, L., Love, D., Reynolds, H., Koichi, K., Chiang, D., Chin, V., Teng, S., Ahmed, M., Henshall, G., Schroeder, V., Lau, J., Nguyen, Q., Maheswari, A., Cannis, J., Clech, J.-P. and Gibson, C., “Reliability evaluation of lead-free SnAgCu PBGA676 components using tin-lead and lead-free SnAgCu solder paste”, Proceedings, SMTA International Conference, Chicago, IL, September 25-29, 2005.
- [23] Bartelo, J., Cain, S. R., Caletka, D., Darbha, K., Gosselin, T., Henderson, D. W., King, D., Knadle, K., Sarkhel, A., Thiel, G. and Woychik, C., "Thermomechanical fatigue behavior of selected lead-free solders", Proceedings, IPC SMEMA Council APEX 2001, Anaheim, CA, Paper # LF2-2.
- [24] Sastry, V. S., Manock, J. C. and Ejim, T. I., “Effect of thermal cycling ramp rates on solder joint fatigue life”, *Journal of Surface Mount Technology*, SMTA, January 2001, pp. 23-28.
- [25] Sharma, P. and Dasgupta, A., “Micro-mechanics of creep-fatigue damage in PB-SN solder due to thermal cycling—Part II: mechanistic insights and cyclic durability predictions from monotonic data”, *ASME Transactions, Journal of Electronic Packaging*, Vol. 124, September 2002, pp. 298-304.
- [26] Yoon, S., Chen, Z., Osterman, M., Han, B. and Dasgupta, A., “Effect of stress relaxation on board level reliability of Sn based Pb-free solders”, Proceedings, 55<sup>th</sup> Electronic Components and Technology Conference, Orlando, FL, May 31 – June 3, 2005, pp. 1210-1214.
- [27] Hall, P. M. und Sherry, W. M., “Materials, structures and mechanics of solder joints for surface-mount microelectronics”, Proceedings, Verbindungstechnik in der Electronic, Deutsche Verband für Schweißtechnik, 3<sup>rd</sup> International Conference,



Fellbach, West Germany, February 18-20, 1986, pp. 47-61.

- [28] Tzan, T., ITRI, Taiwan, private communication.
- [29] Norris, K. C. and A. H. Landzberg, A. H, "Reliability of Controlled Collapse Interconnections," *IBM Journal of Research and Development*, May 1969, pp. 266-271.
- [30] Itoh, M., Sakai, Y., Miwa, M. and Taketomi, K., "Direct mounting of chip carriers on printed wiring board", NEC Research and Development, No. 65, April 1982, pp. 33-38.
- [31] Vandeveld, B., Beyne, E., Zhang, K., Caers, J., Vandepitte, D. and Baelmans, M., "Parametrized modeling of thermomechanical reliability for CSP assemblies", *ASME Transactions, Journal of Electronic Packaging*, Vol. 125, No. 4, December 2003, pp. 498-505.
- [32] Yang, H., Elenius, P., Barrett, S., Schneider, C., Leal, J., Moraca, R., Moody, R., Kweon, Y-D., Patterson, D. and Goodman, T., "Reliability characterization in Ultra CSP™ package development", Proceedings, 50th Electronic Components and Technology Conference, Las Vegas, NV, May 21-24, 2000, pp. 1376-1383.

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